Sustainable Additive Manufacturing of Electronics and 3D Heterogeneous Integration for Advanced Packaging

Ahmed Busnaina, William Lincoln Smith Professor, Distinguished University Professor and Director of the NSF Nanoscale Science and Engineering Center for High-rate Nanomanufacturing, Northeastern University, Boston, MA

www.nanomanufacturing.us, www.nano-ops.us

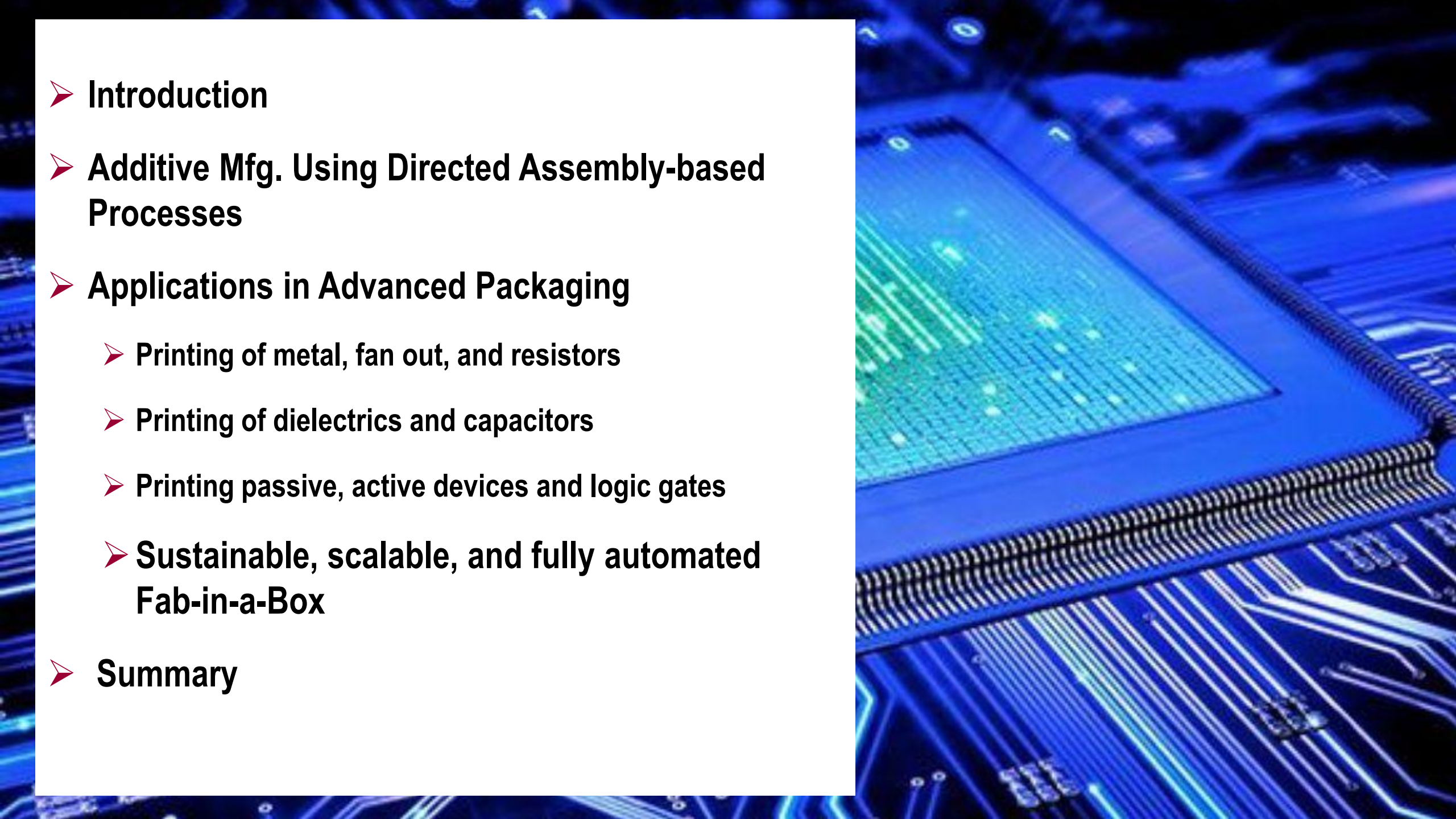
What if?

- There is an electronics manufacturing technology that can reduce costs by 10-100%.
- Reduces the carbon footprint by more than one order of magnitude?
- Imagine if such a technology does not use any corrosive or toxic chemicals.

Such a technology exists.

This will be the topic of my presentation.

Semiconductor Foundry in a Box



- Introduction
- Additive Mfg. Using Directed Assembly-based Processes
- Applications in Advanced Packaging
  - Printing of metal, fan out, and resistors
  - Printing of dielectrics and capacitors
  - Printing passive, active devices and logic gates
  - Sustainable, scalable, and fully automated Fab-in-a-Box
- Summary

The Challenges Facing the Electronics Industry Today

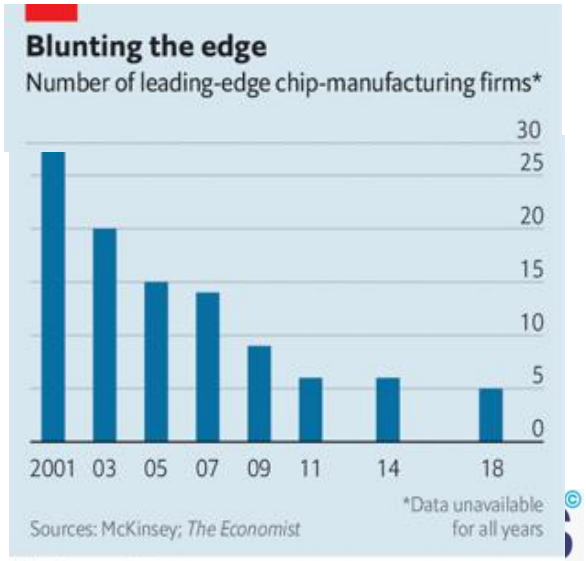
Financial and Environmental Cost

Commercial electronics manufacturing is expensive, with plants costing up to **$20 billions each** and one billion per year to operate, in addition to using massive amounts of power, water and chemicals.

1990s cost ~ $1B

2025 cost ~ $20-$40 B

- A typical fabrication plant uses as much power in a year as 50,000 homes.
- It takes six to eight weeks to make a processor chip (memory chips take longer).



What if we A Sustainable Semiconductor Foundry in a Box

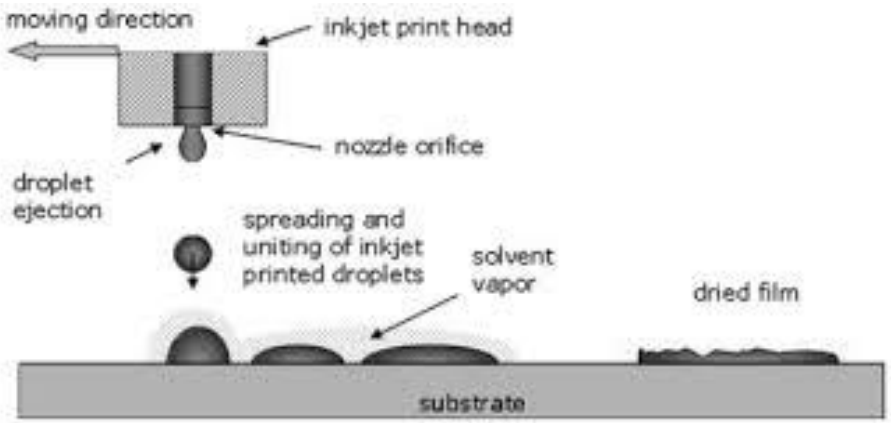
- On-demand chips in a few hours
- No etching, chemical reactions, or vacuum
- Reduces carbon footprint by more than an order of magnitude
- 100 times less cost
- 100 times faster than conventional fabrication
- A 1000 times reduction in materials use
- 1000 times faster than 3D printing
- 25 nm to 1000 microns feature size demonstrated
- eliminating 100s of process steps

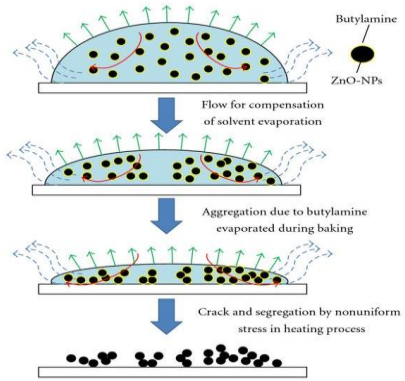
Semiconductor Foundry in a Box

Patented new technology (directed assembly-based printing) to print circuits at the nano and microscale funded by NSF and DoD.

How does directed assembly-based printing work?

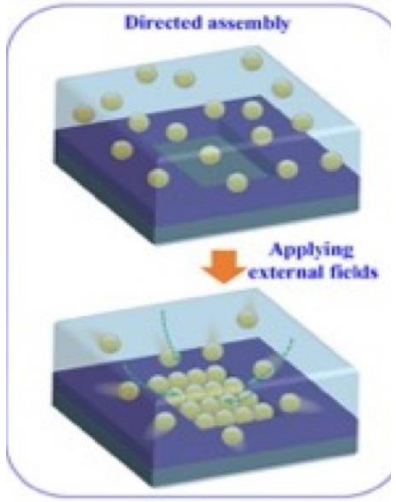
Inkjet printing

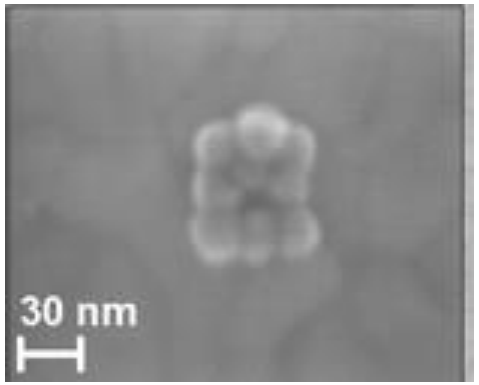




- **Directs a droplet** toward a substrate to form a pattern using many (dots) limiting pattern resolution and fidelity.
- Inherently relies on mechanical accuracy.
- Materials limited to organics and metals

Directed assembly-based printing



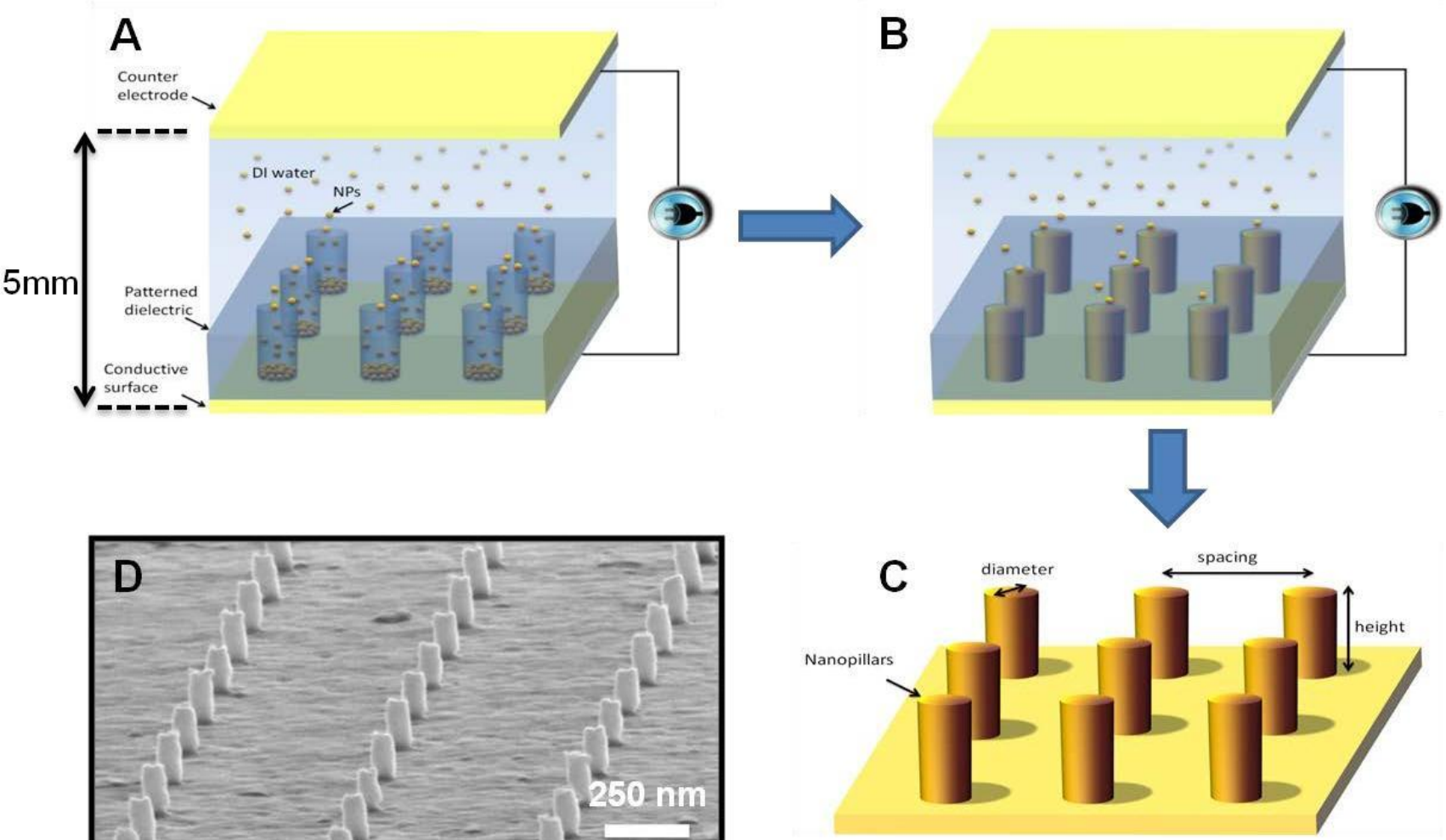


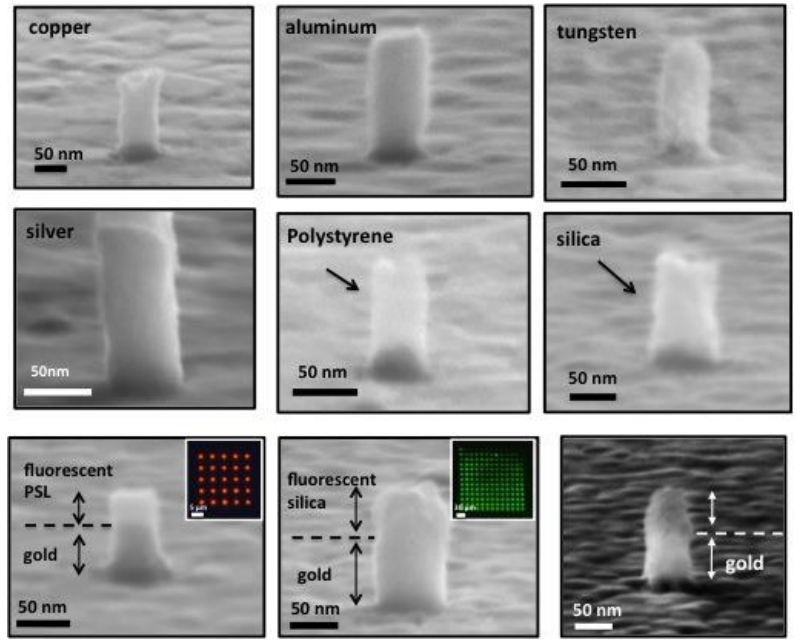
- **Directs each nanoparticle** (down to 3nm in size) toward a substrate to form a nanopattern.
- Prints 1000 times faster & smaller patterns than inkjets
- Prints one circuit layer per minute

NanoOPS©

Electrophoretic Directed Assembly– EPx Platform

Assembled Interconnects

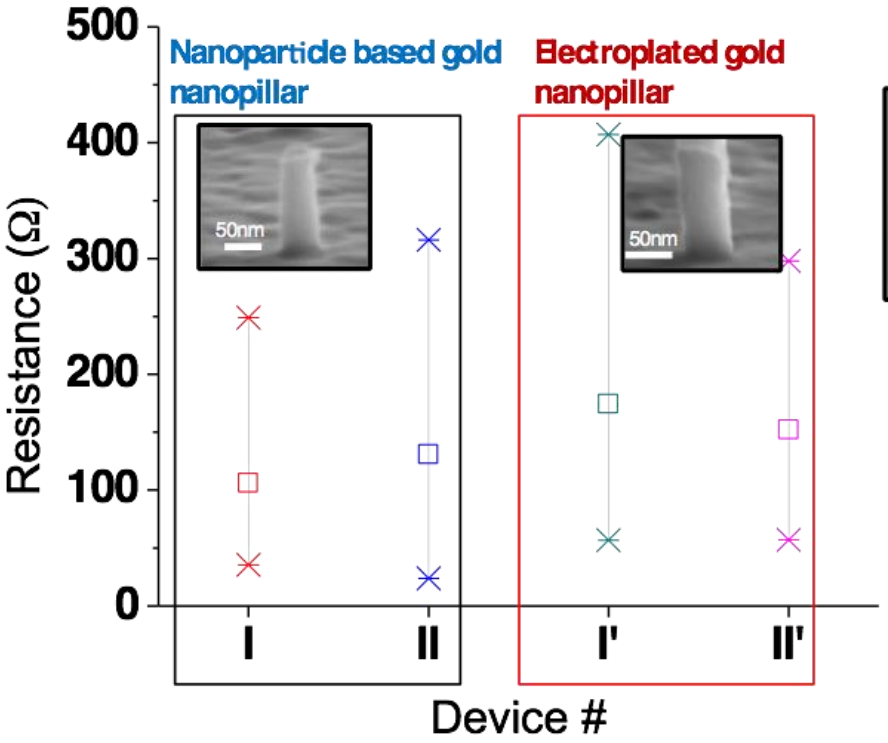


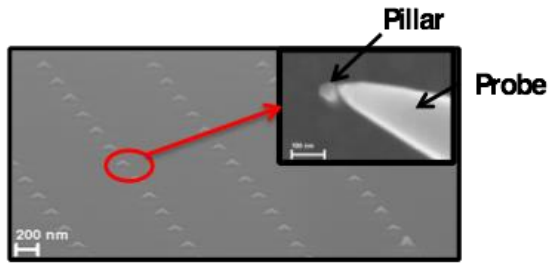


All assembled Nanoparticles are completely fused insitu.

ACS Nano, 8 (5), 2014.

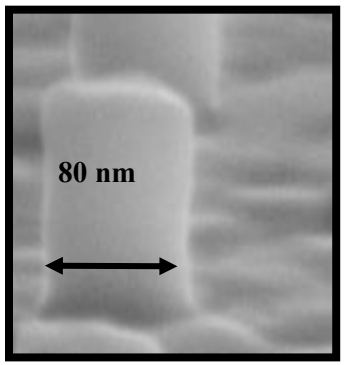
Interconnects Properties

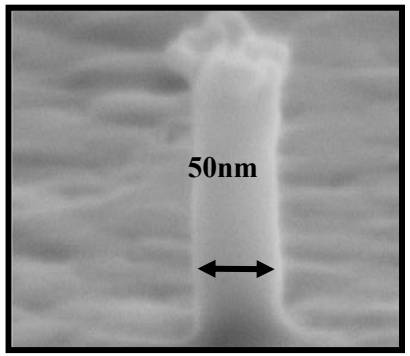


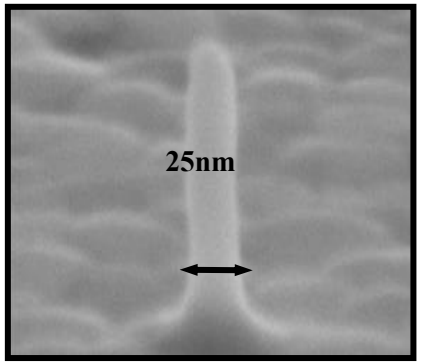


Resistance of assembled interconnects is the same as bulk (electroplated interconnects).

Crystalline Au Pillars



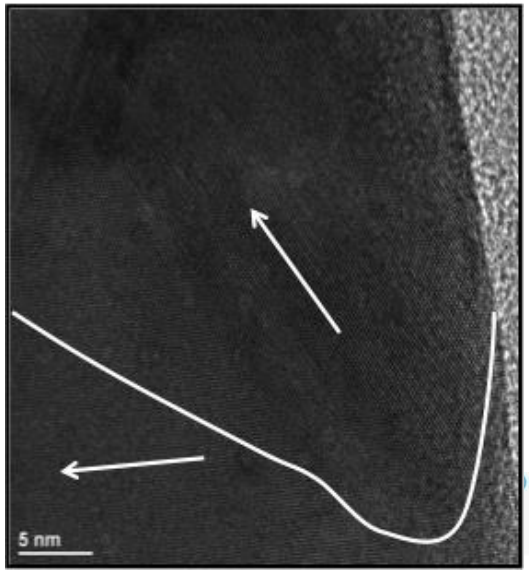




Directly assembled structures properties are equivalent to electroplating, CVD and PVD fabrication.

Directly assembled metallic structures (Cu, Ag, Al, Au, and W, etc.) in addition to semiconductors and dielectrics were demonstrated.

- TEM shows that NPs completely fuse without any voids at room temperature.
- Nanopillars have polycrystalline nature.



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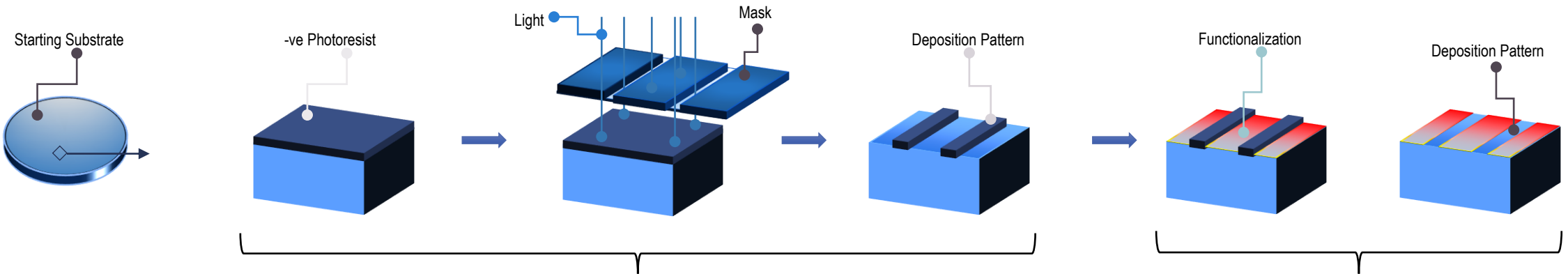
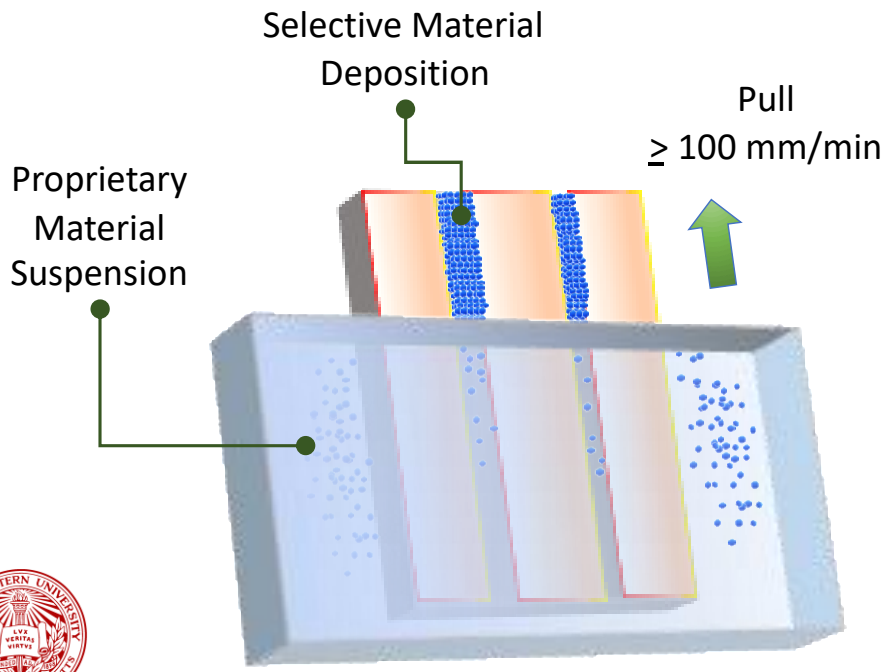
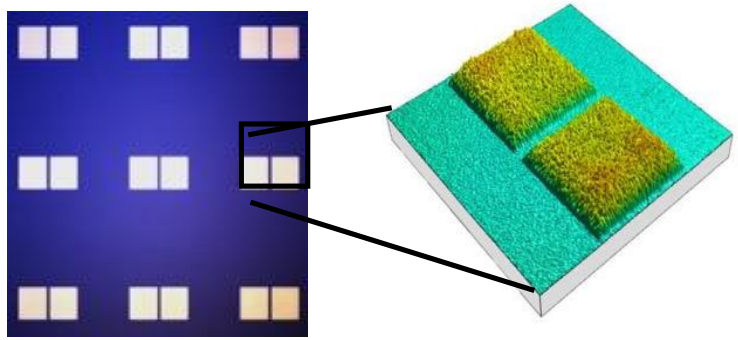
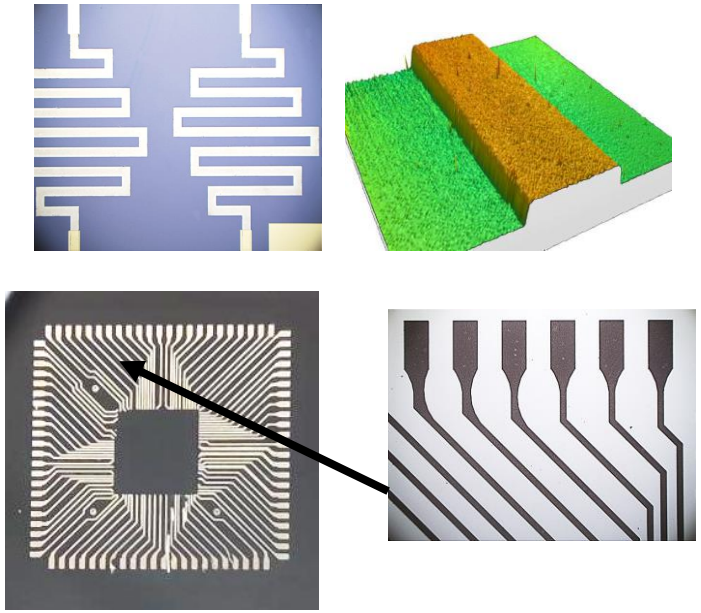
Fast Fluidic Assembly Process– FFx Platform





SiO_2 substrate – 10 µm spacing





Fast Fluidic Assembly Process

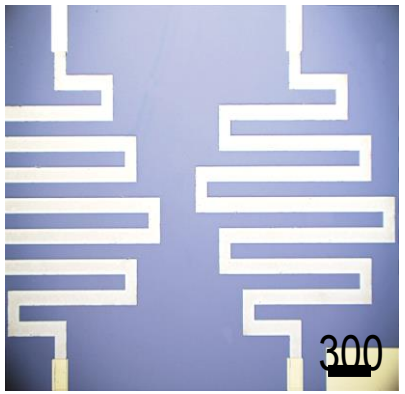
What inorganic materials were additively manufactured and utilized?

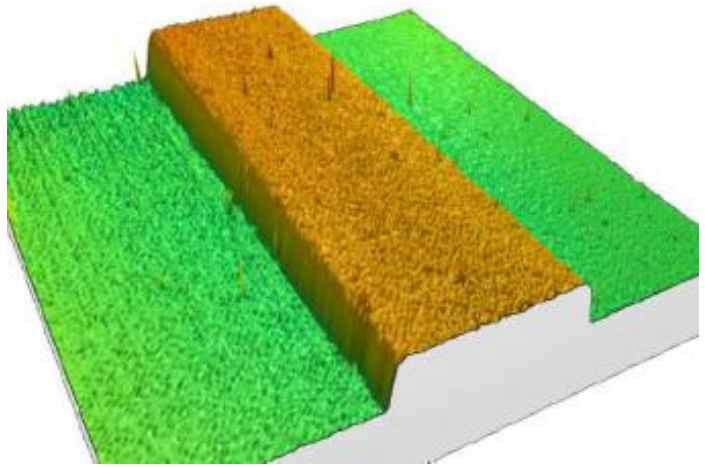
Material Type	Material	Made nano & micro structures	Sintered at room temp	Sintered at High temp	Devices made & tested
Conductor	silver	yes	yes	yes	passive & active
	copper	yes	yes	yes	passive & active
	gold	yes	yes	yes	passive & active
	platnium	yes	no	yes	passive
	alumnium	yes	yes	no	no
	Tungesten	yes	yes	no	no
Semiconductor	Silicon	yes	yes	yes	passive & active
	ZnO	yes	no	yes	active
	ZnSe	yes	yes	yes	active
	InP	yes	no	yes	no
	GaAs	yes	no	no	no
	GaN	yes	no	no	no
Dielectric	SiO2	yes	yes	yes	passive & active
	Alumina	yes	yes	yes	passive & active
	HfO2	yes	yes	yes	passive & active
dopants	B+	yes	no	yes	passive & active
	P-	yes	no	yes	passive & active

Nano OPS©

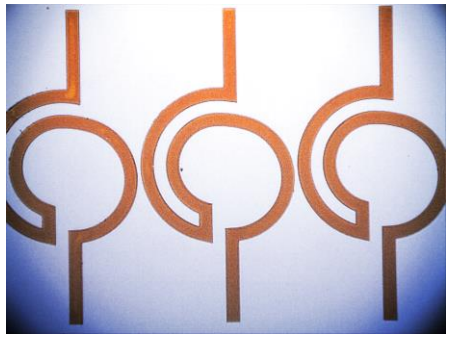
Profile of Metal Lines

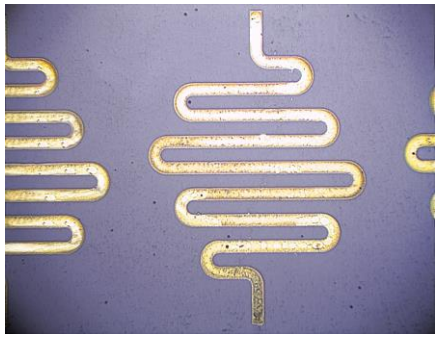
- Confocal microscope measurements show an average platinum thickness of 250 nm after annealing using RTP at 800 °C for 2 mins .

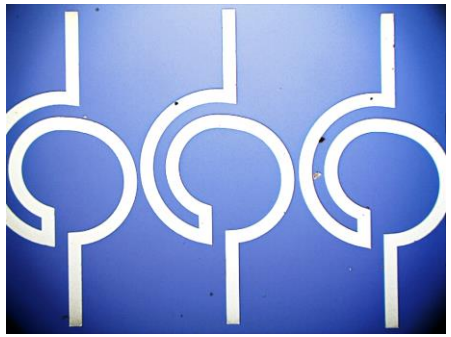


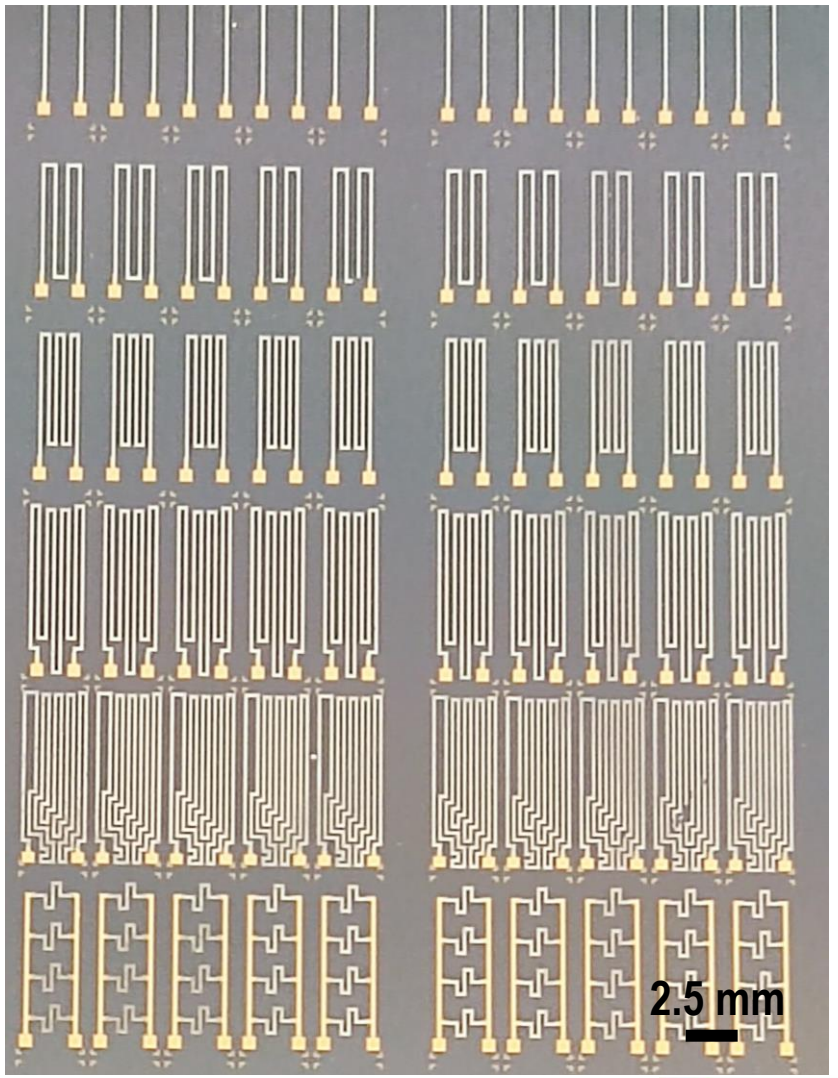


The printed Platinum shows uniform and homogeneous surface morphology.


Copper


Gold


Platinum



50 Ω

100 Ω

250 Ω

550 Ω

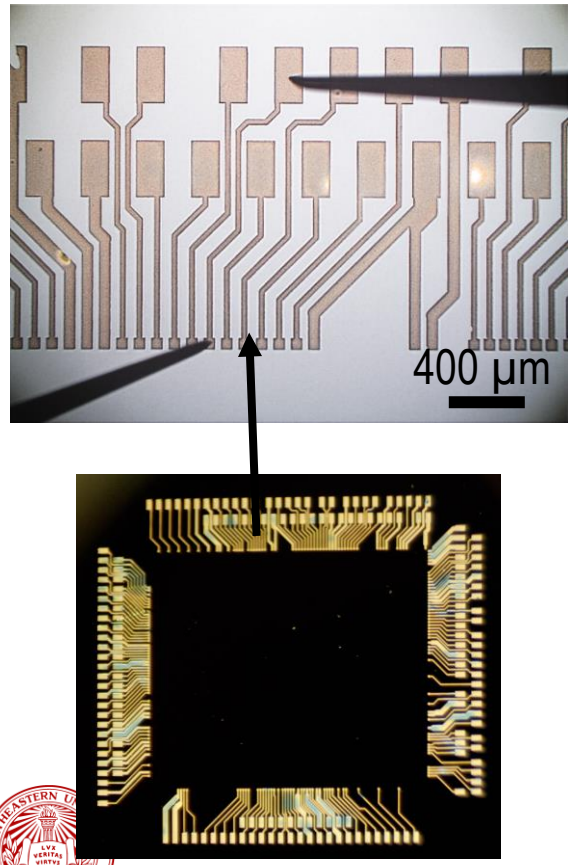
800 Ω

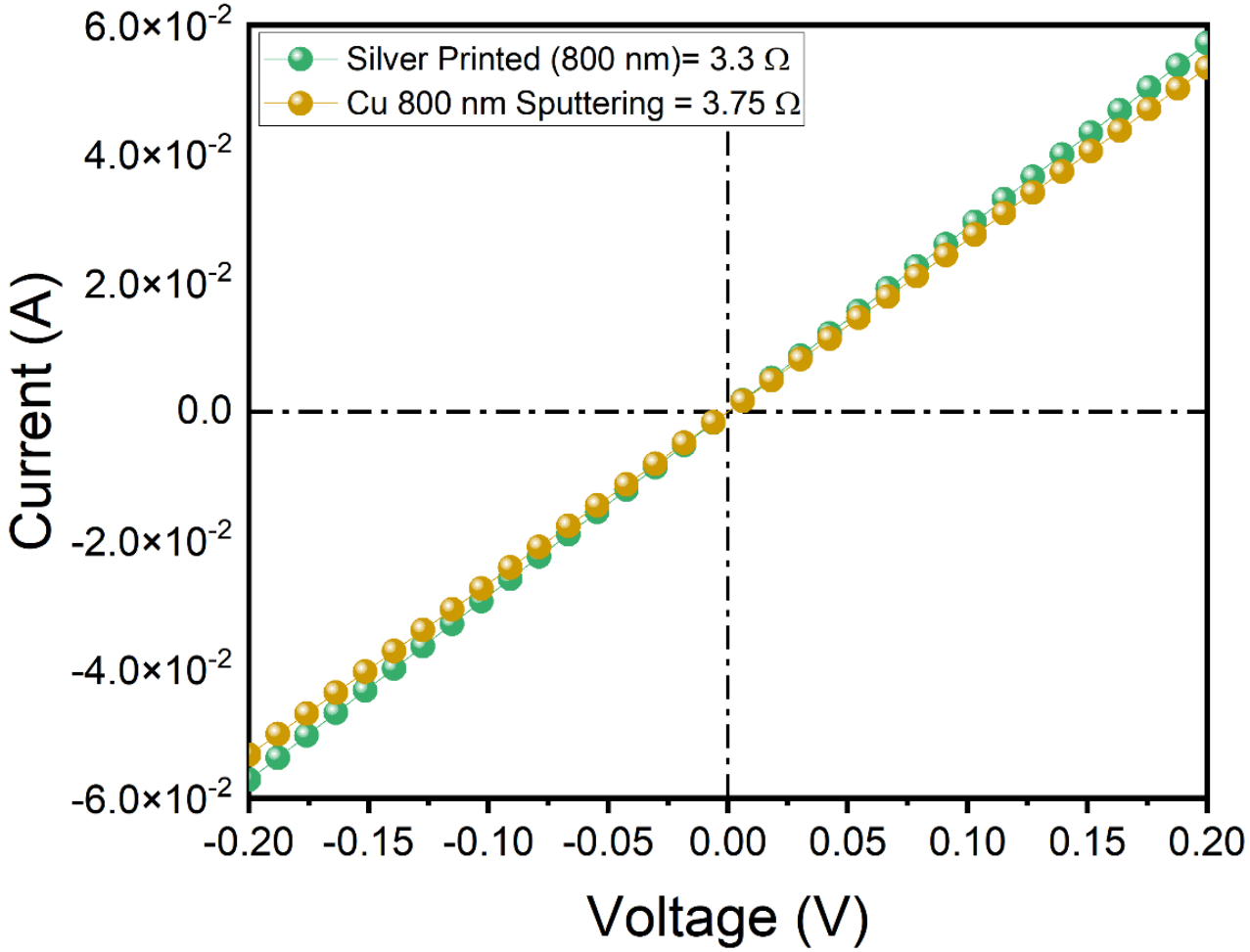
30 Ω

Additively Manufactured Silver vs Sputtered Copper

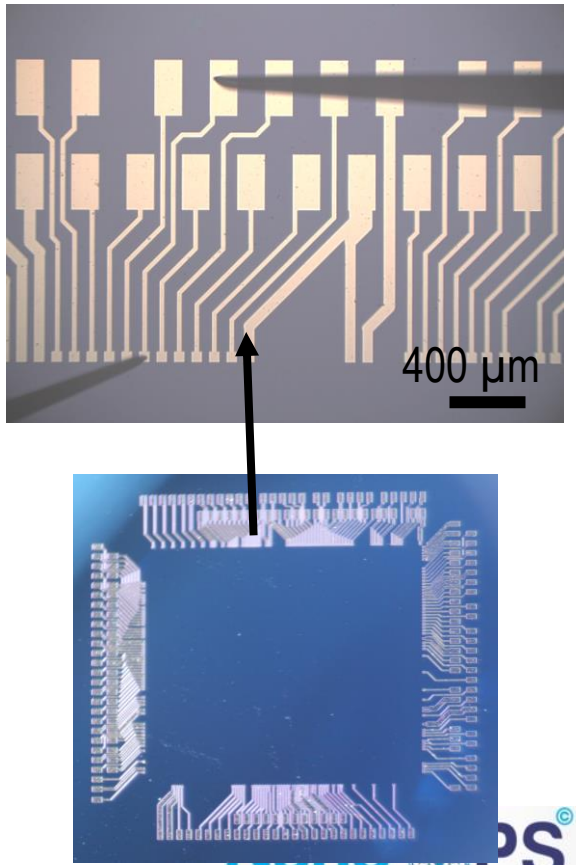
- Fan out Flip chip pattern was made using silver (internal pads < 40 microns)
- The trace's conductivity is equivalent to sputtered copper at the same thickness.

Silver



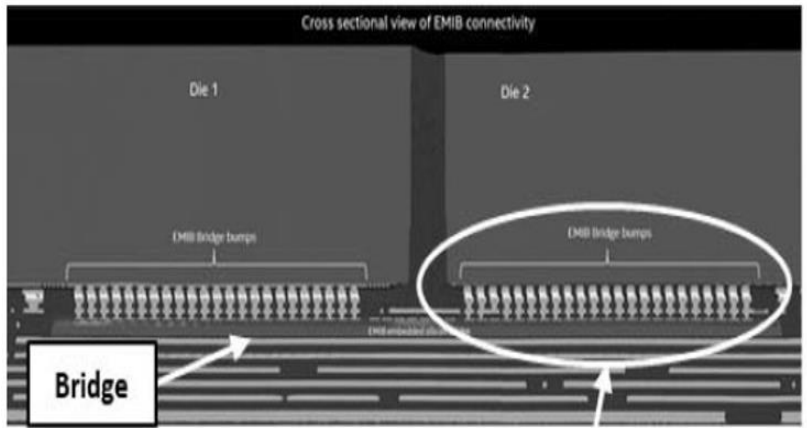


Copper (sputtered)

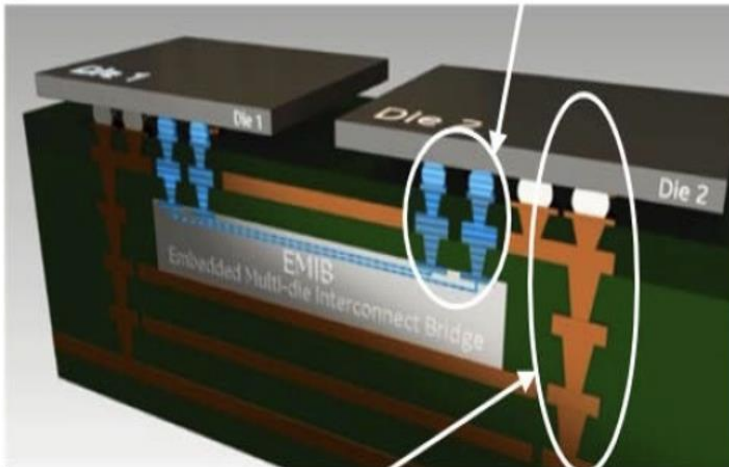


Additively Manufactured EMIB-Like Structures

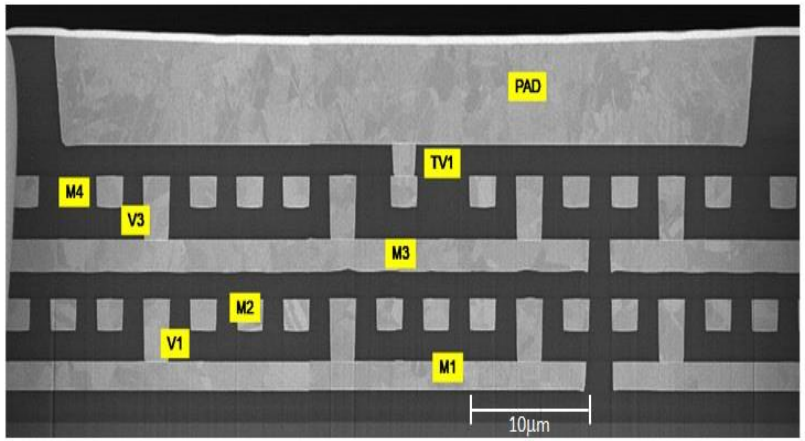
- Intel's Embedded Multi-die Interconnected Bridge (EMIB) is an advanced chip packaging technique connects multiple heterogeneous dies or chiplets within a single package.
  - More compact than a large silicon interposer



Localized Fine Pitch Interconnects used for die-to-die interconnects

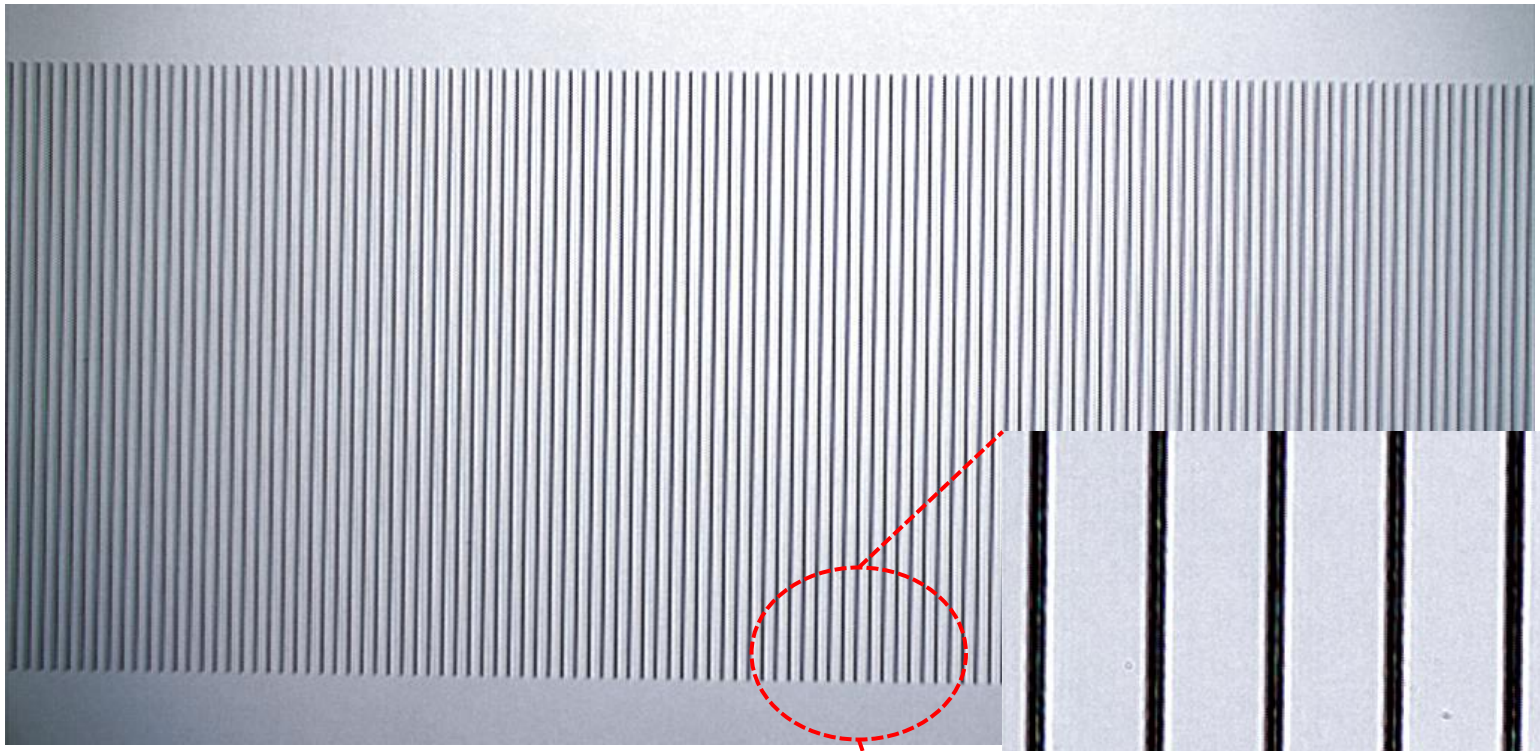


Package interconnects outside of the bridge region are unaffected

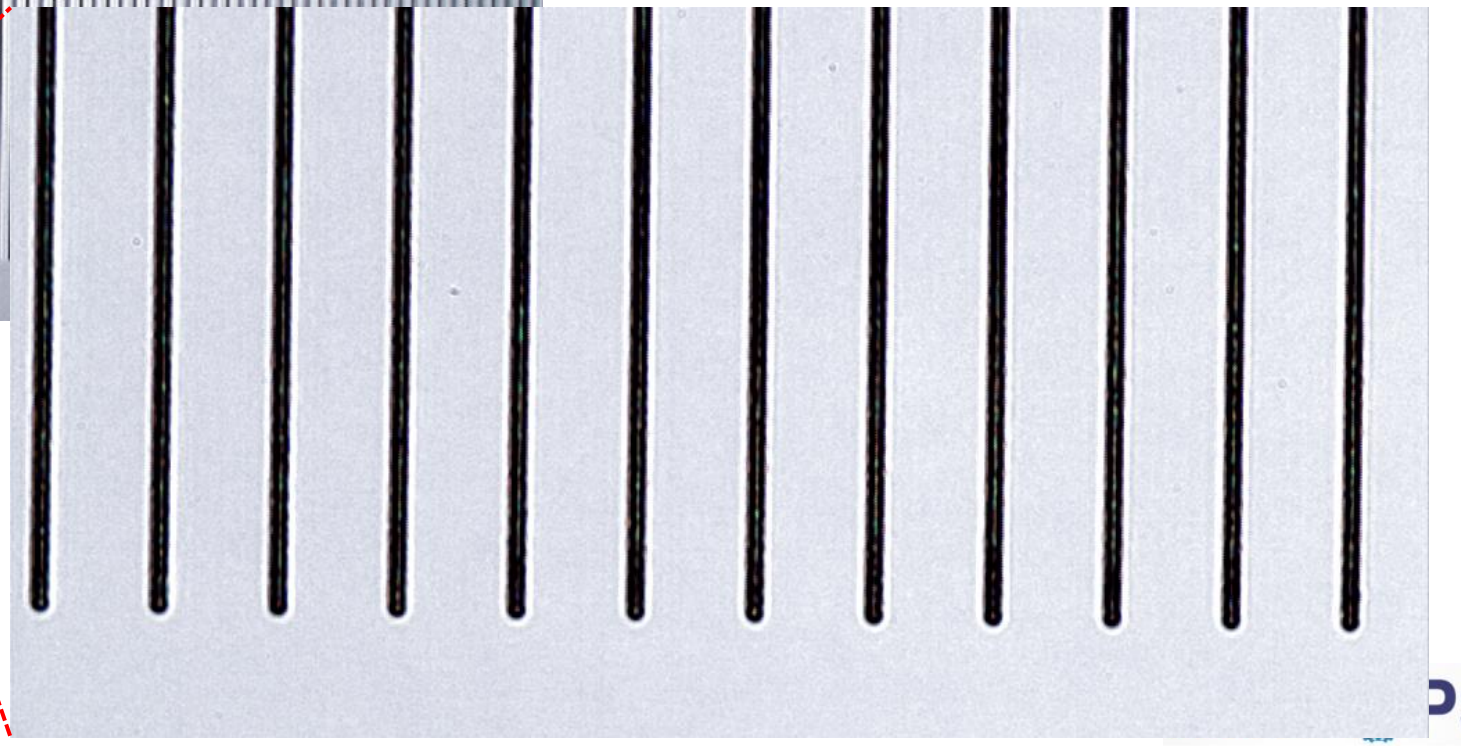


Bridge Cross-Section showing 4 Metal layers with 2 µm Lines/Spaces/vias.

Additively Manufactured EMIB-Like Structures



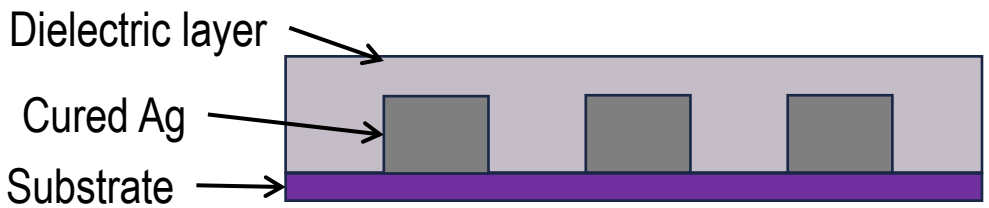
Two micron lines (trace) with 100, 500, and 1000 um lengths are fabricated with four different spacings: **2, 4, 10, and 20 um.**

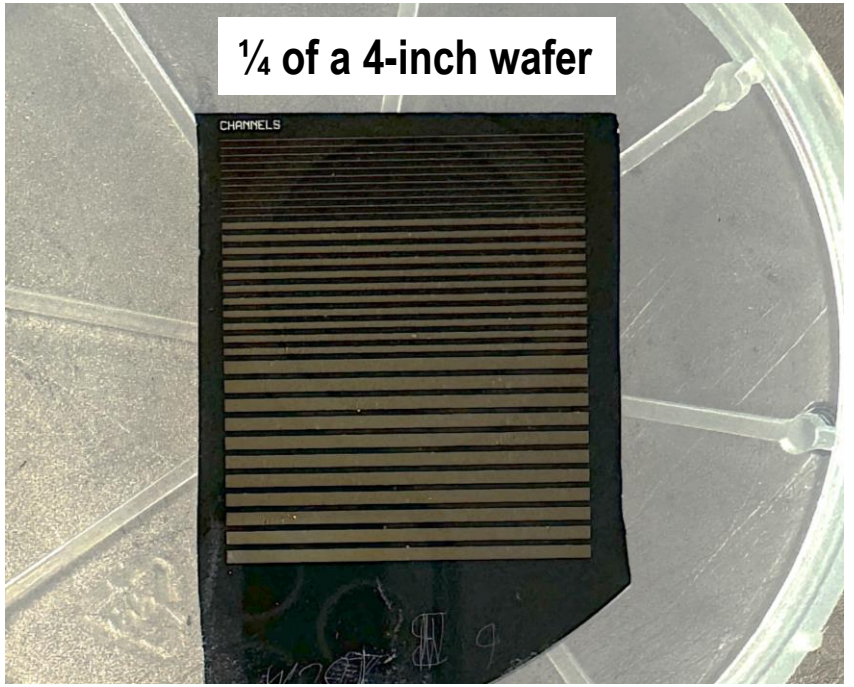


1000 um length
2 um linewidth
20 um spacing
~0.5 um thickness

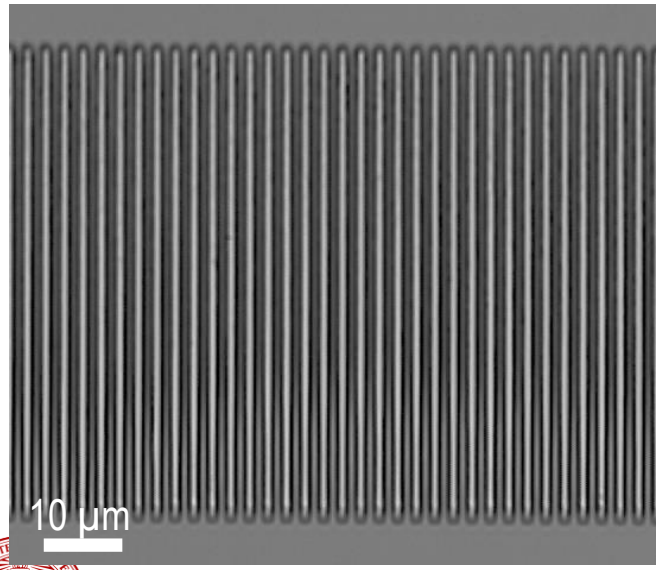
Additively Manufactured EMIB-Like Structures

- **Printed pitch: 4, 7, 12, and 22 µm**
- The width of each line is 2 µm
- Three-different lengths: 100, 500, & 1000 µm

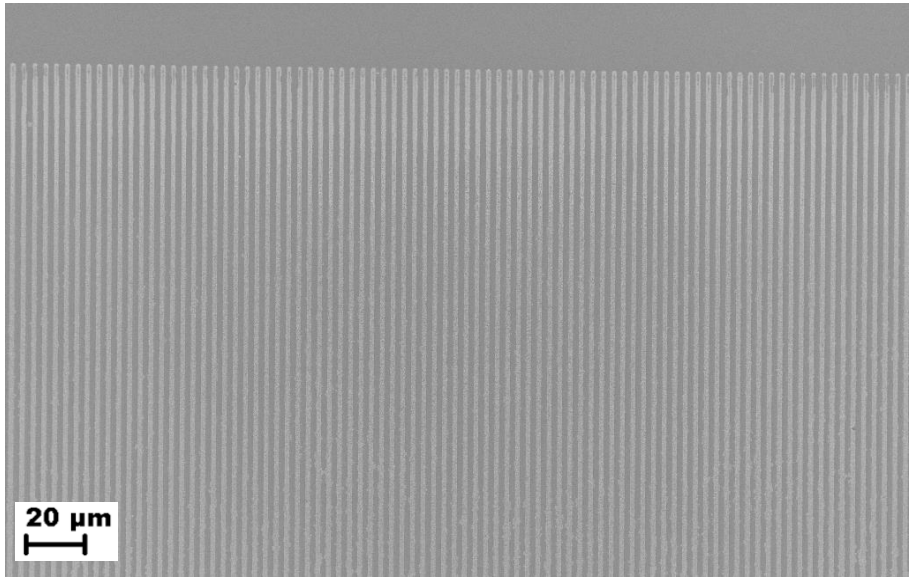




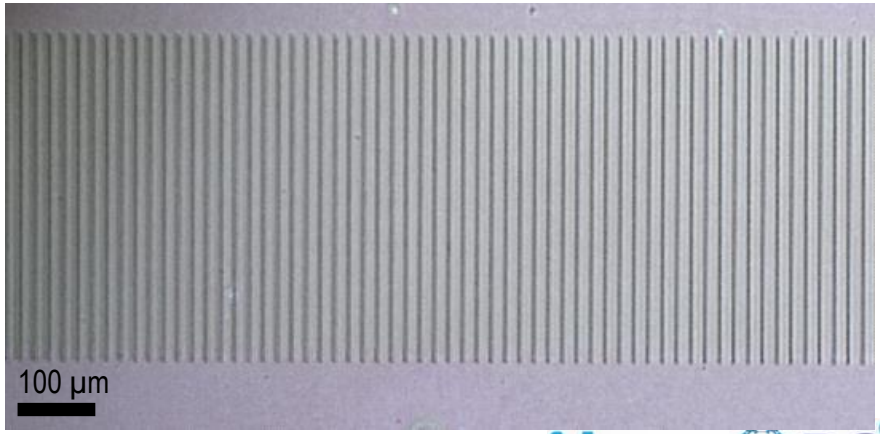
50 length-to-width aspect ratio



500 length-to-width aspect ratio with **4 µm pitch**

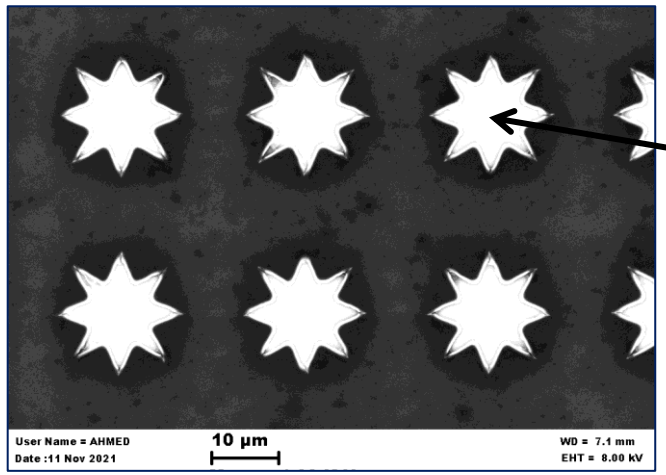


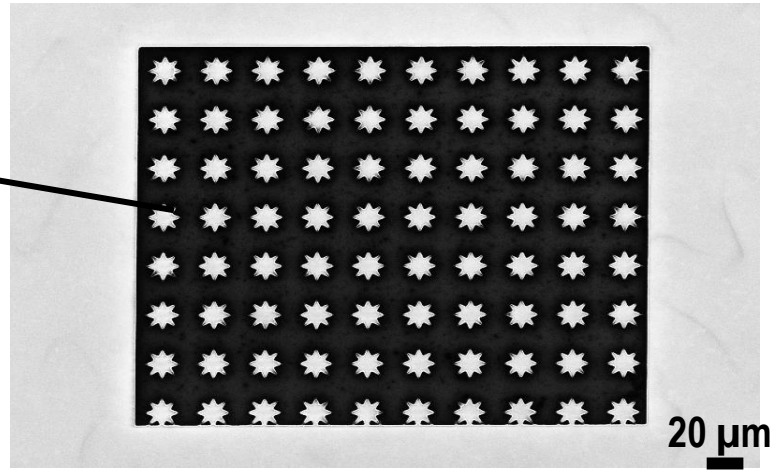
250 length-to-width aspect ratio



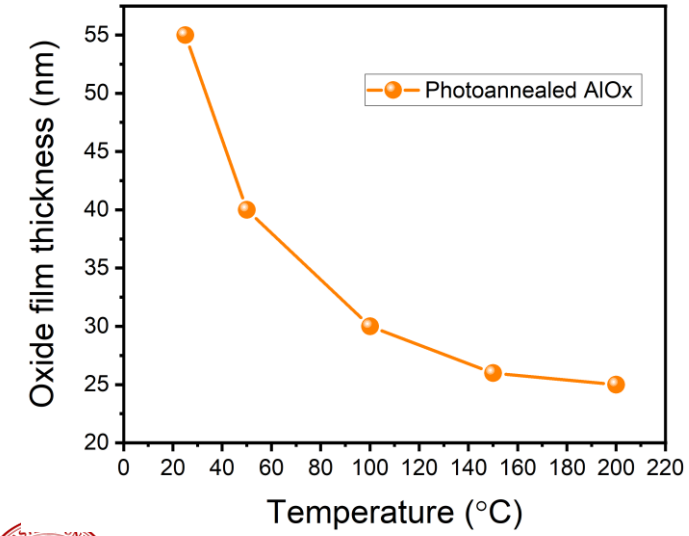
Additively Manufactured Dielectrics

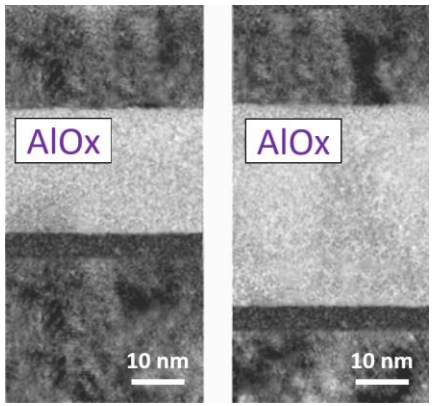
The SEM images below shows Al_2O_3 micropatterns prepared by directed fluidic assembly with a dielectric constant that matches that obtained by CVD or ALD ($\varepsilon_d = 7.2$).

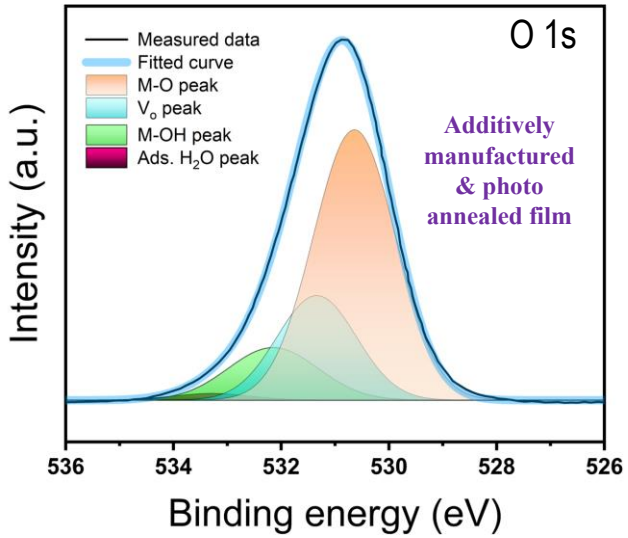


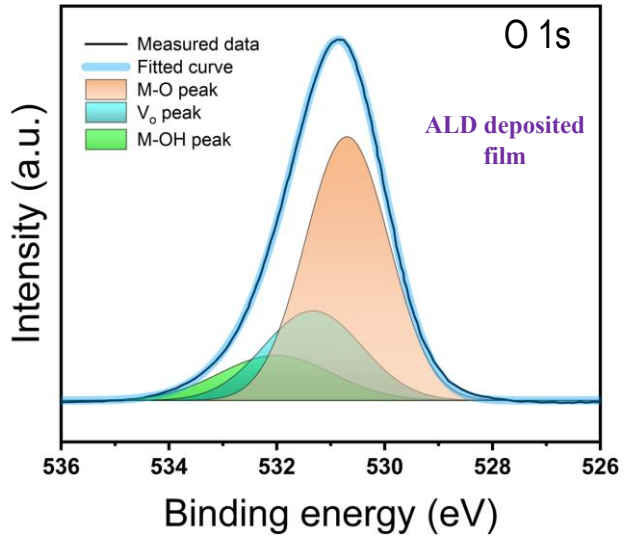


X-ray Photoelectron Spectroscopy (XPS) characterization of the Dielectric Layer shows agreement in between ALD and printed films in terms of peak intensities and composition ratios.



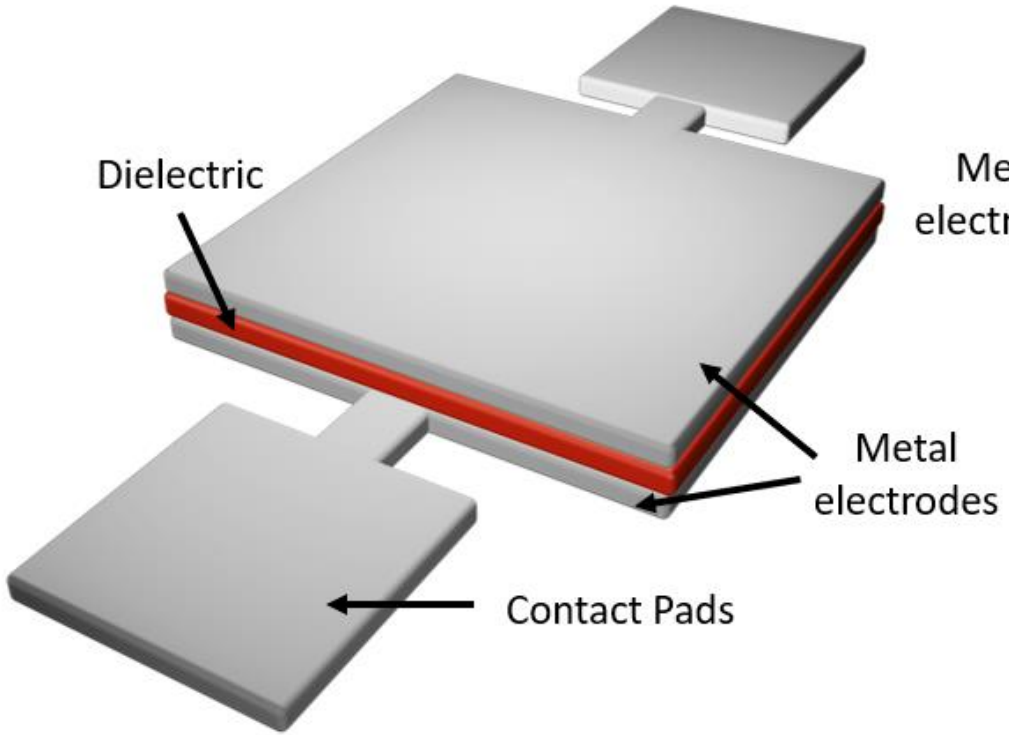


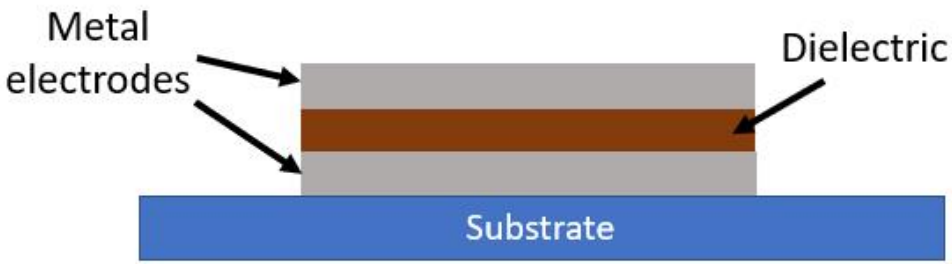


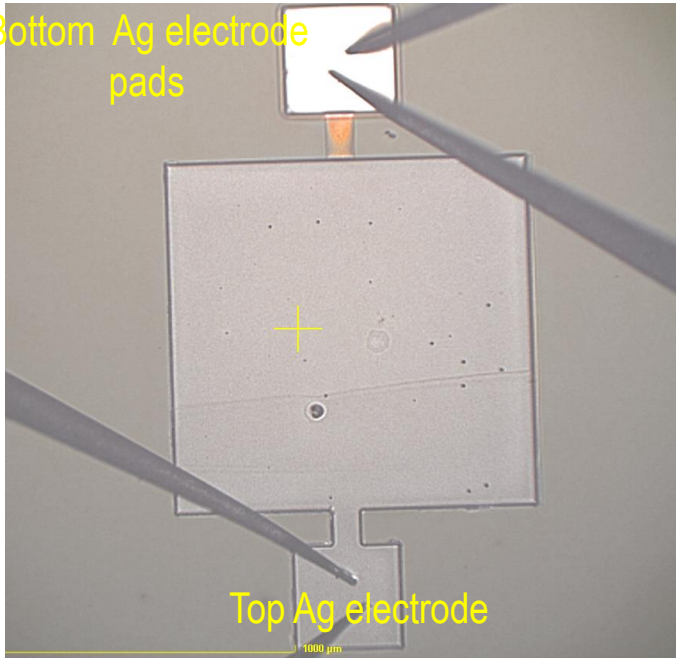


- Higher temperature densification and better dielectric properties for the film.
- Cross-sectional shows the oxide film thickness variation between 50 °C and 200 °C annealing.

Additive Manufacturing of Capacitors



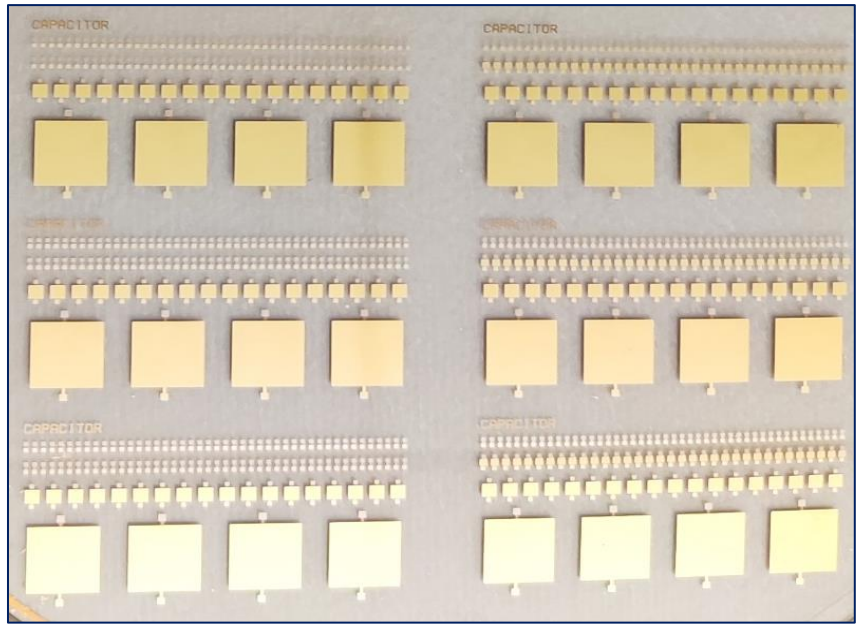




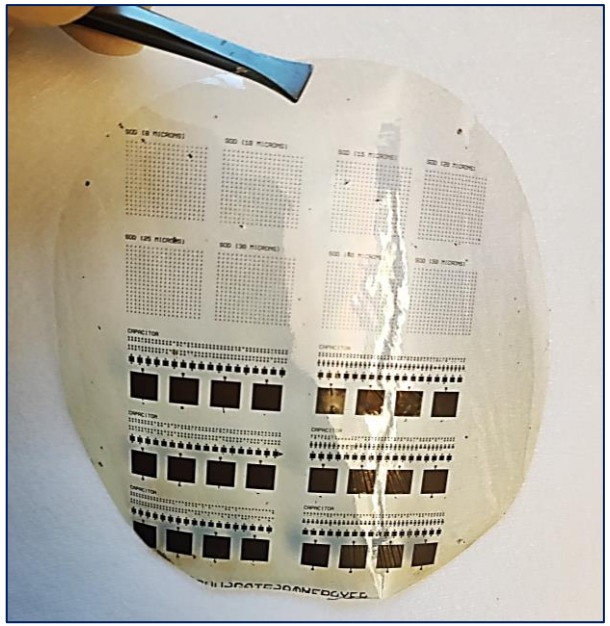
Additively Manufactured Capacitors on Rigid and Flexible Substrates

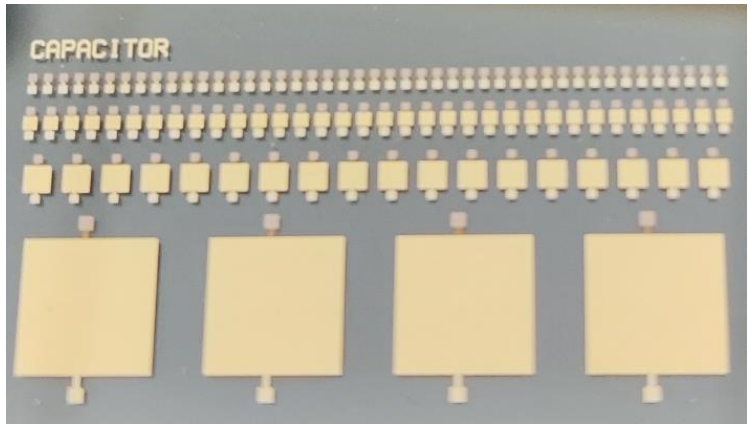
- Large-scale fabricated capacitors with a dielectric layer onto sapphire or polymer substrates.
- Each substrate has 640 capacitors with different surface areas of side lengths 20, 50, 100, 500, 1000, and 5000 µm.
- Metal: **Silver**
- Dielectrics: **Al_2O_3, SiO_2, HfO_2**

Capacitors on a sapphire substrate

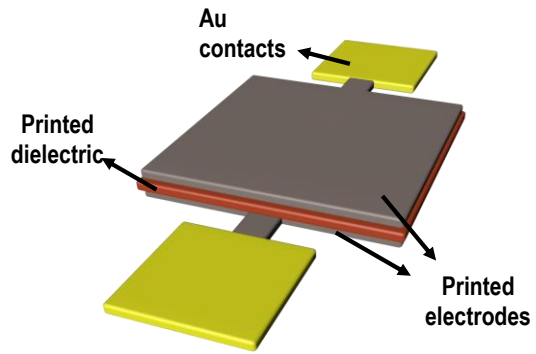


Capacitors on a polymer



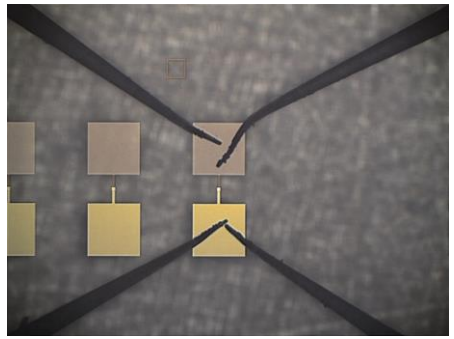


Capacitors on silicon



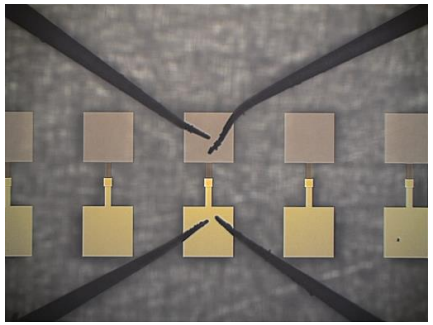
Characterization of Additively Manufactured Capacitors

- For high-frequency applications, the capacitors need to show reliable performance under high frequency.
- The curve shows the capacitance variation versus different frequencies up to 1 MHz.



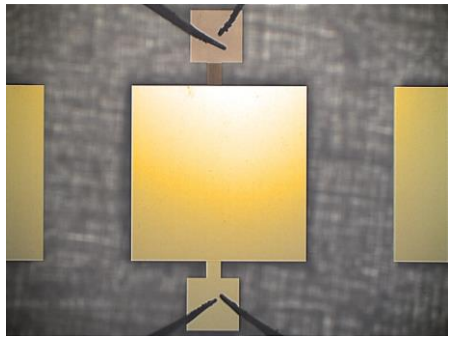
20x20 µm

C= 857 fF



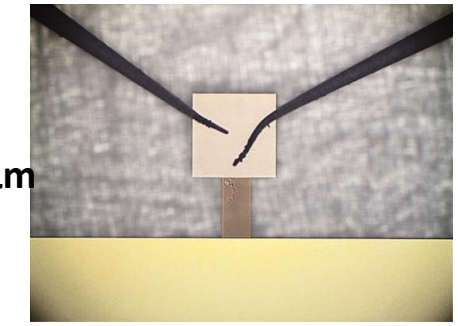
50x50 µm

C= 4.3 pF



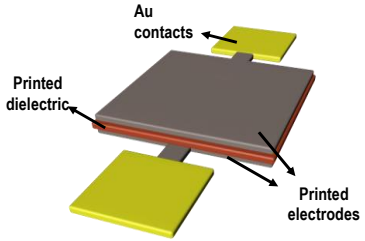
1000x1000 µm

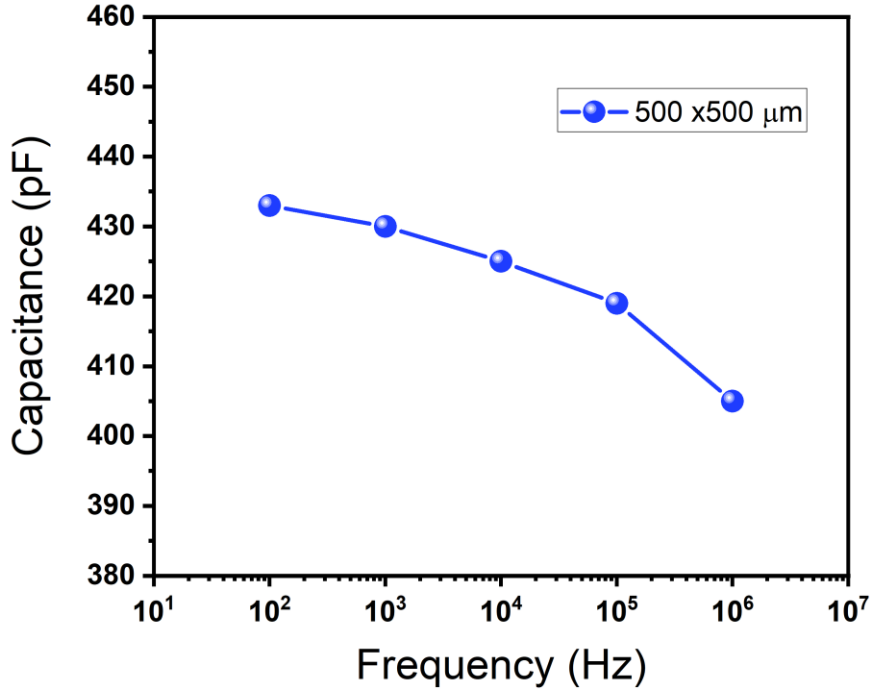
C= 1.6 nF

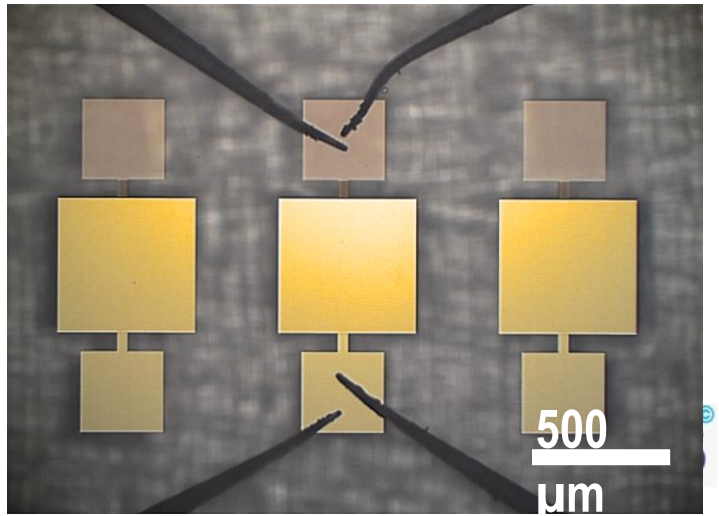


5000x5000 µm

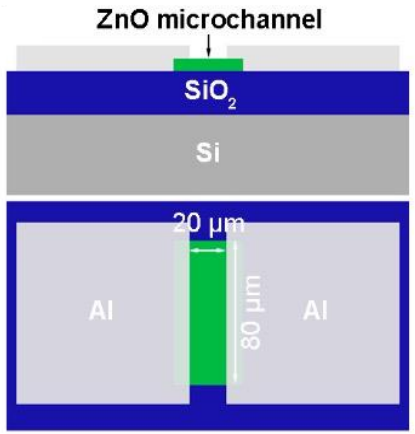
C= 5.68 nF

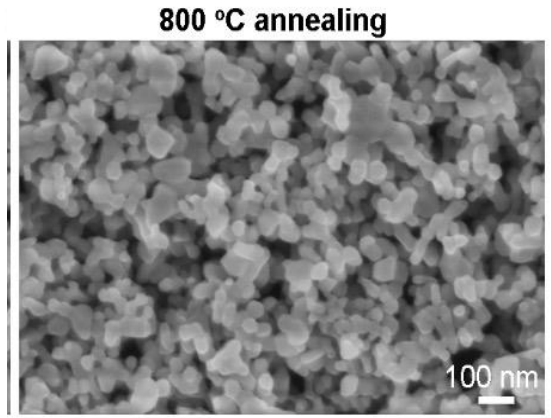


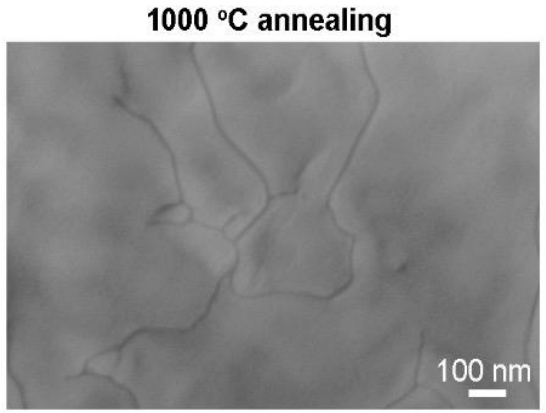


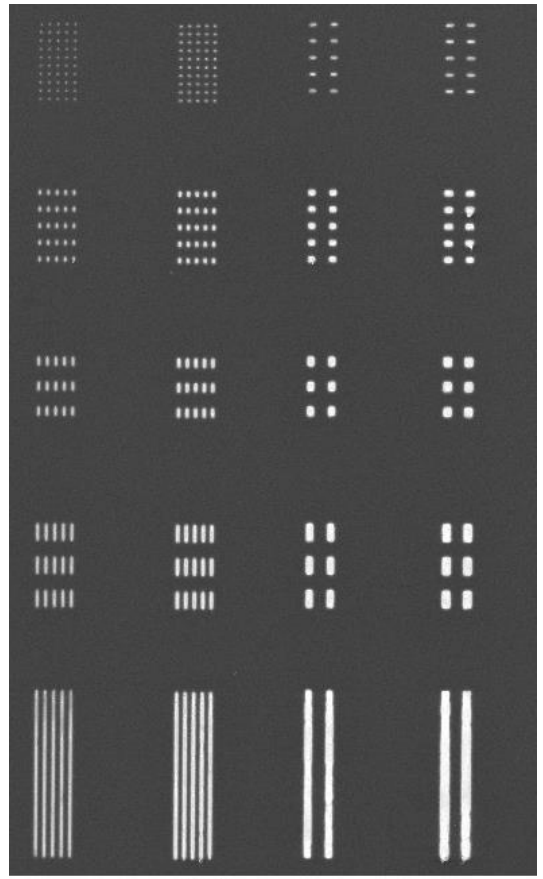


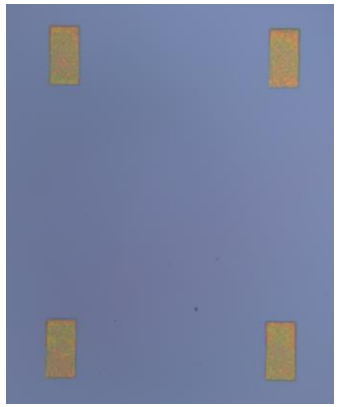
Field Effect Transistor (FET) Using II-VI Semiconductors



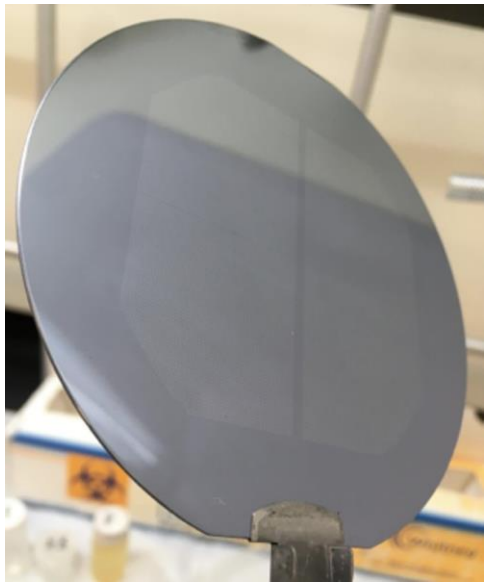


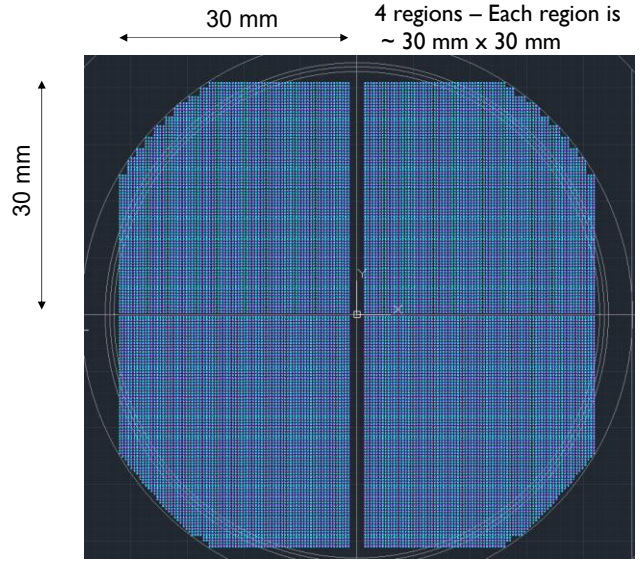


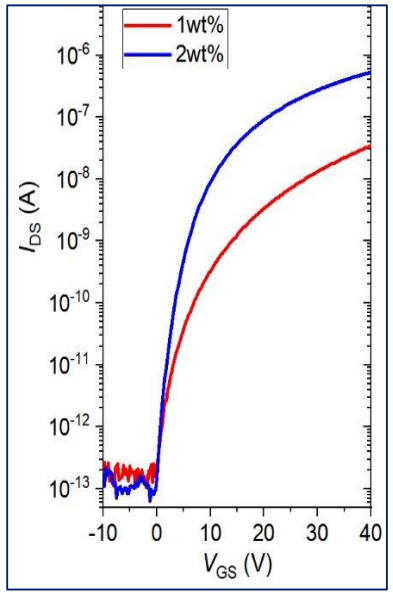




Channel width varied from 100 nm to 2 um, length varied from 100 nm to 20 um



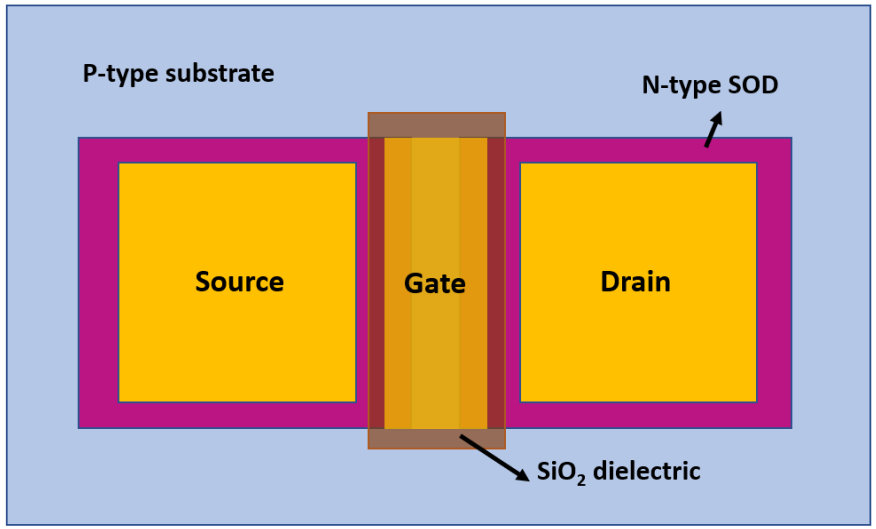




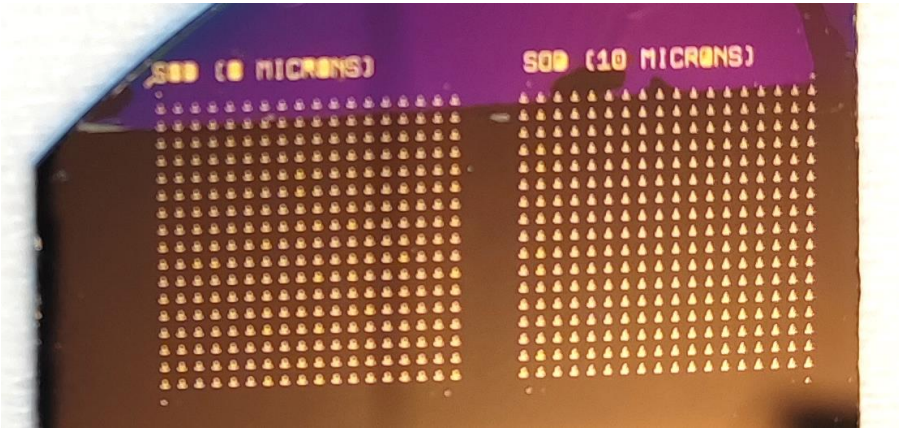
Wafer-level manufacturing of 37,000 transistors exhibiting an on/off ratio higher than 10^6 after annealing.

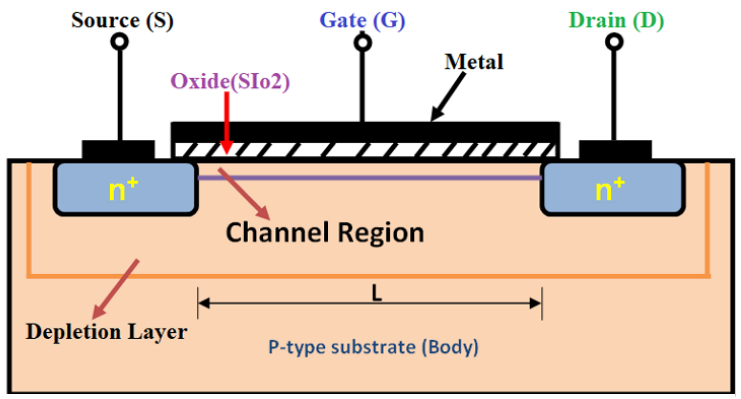
ACS Applied Electronic Materials, 2023

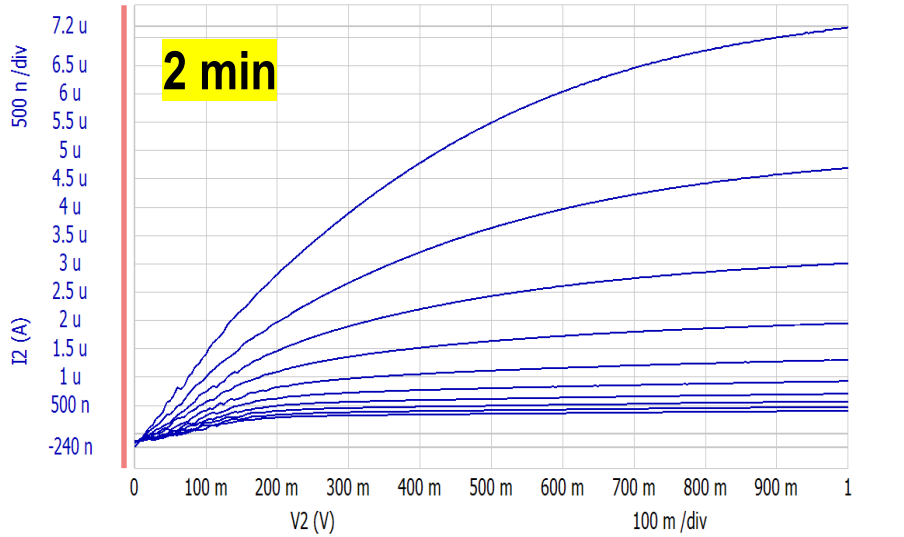
Additively Manufactured Silicon Transistors (MOSFETs)

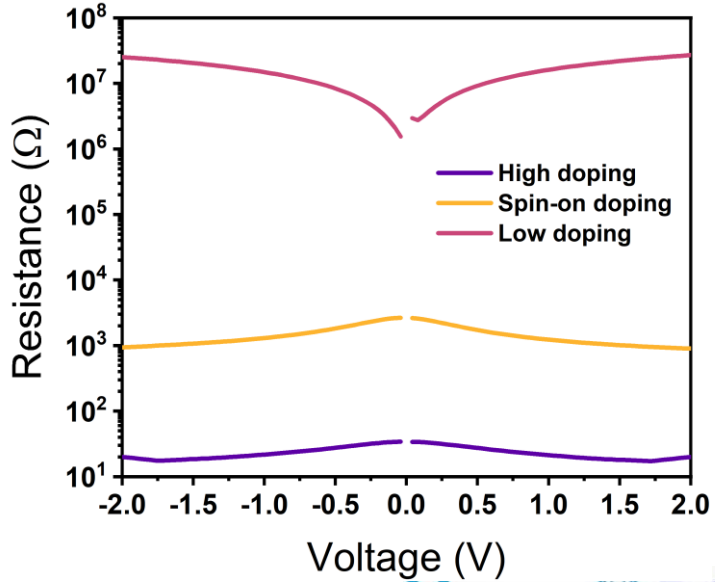


A fully additive liquid-based process process to manufacture MOSFETs using dopants inks.



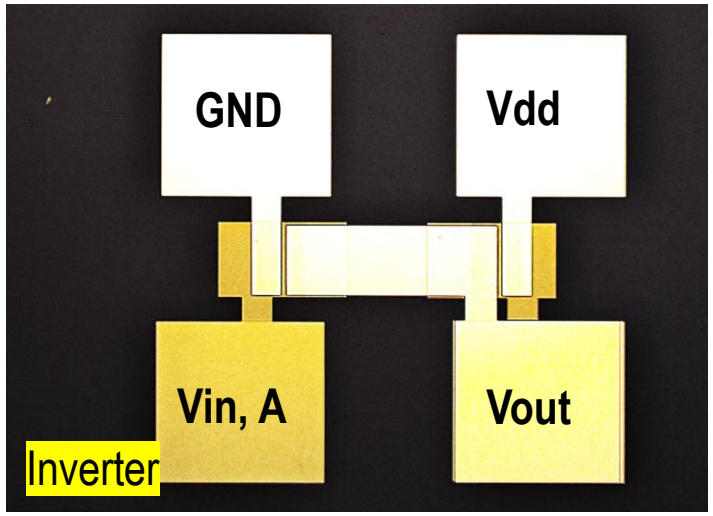


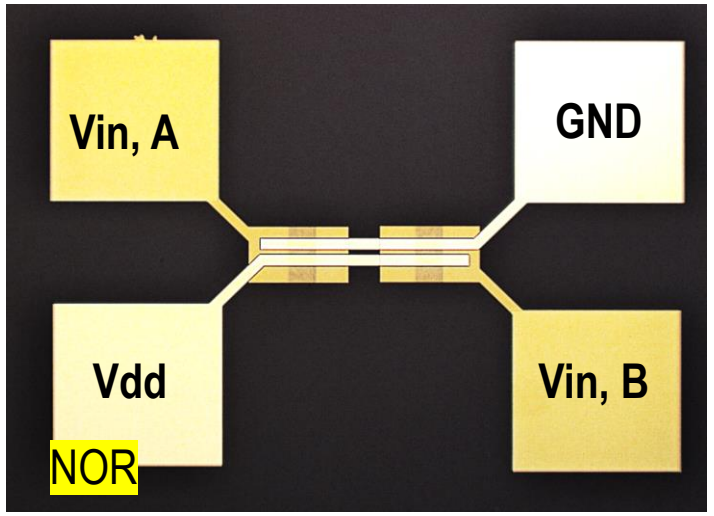


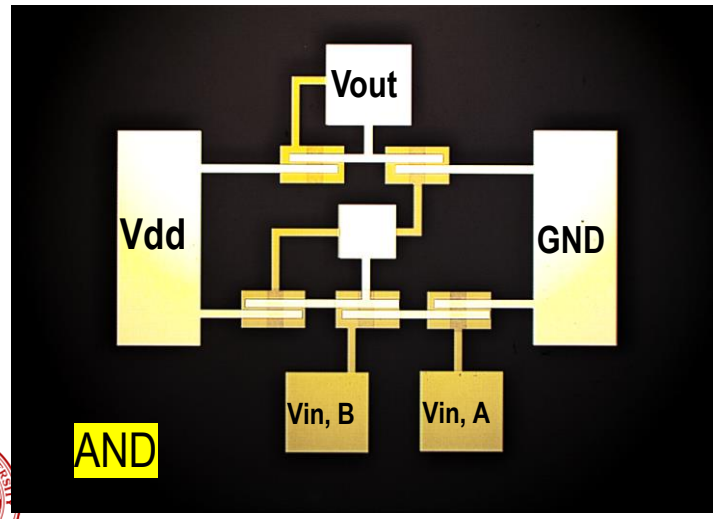


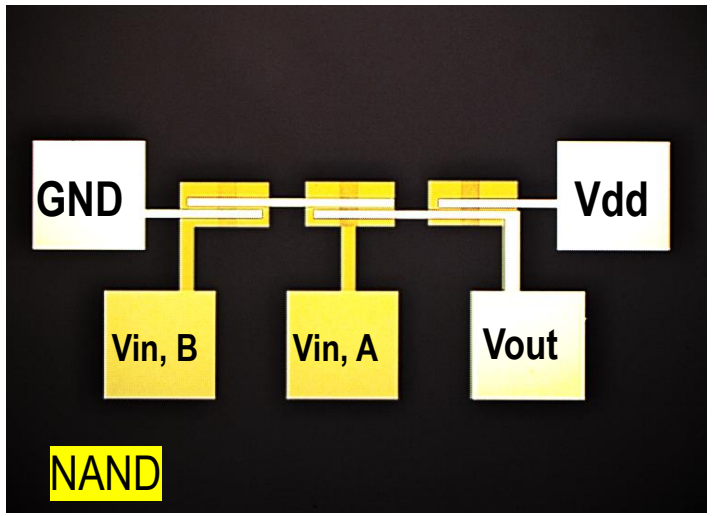
Additively Manufactured Logic Gate Electronics

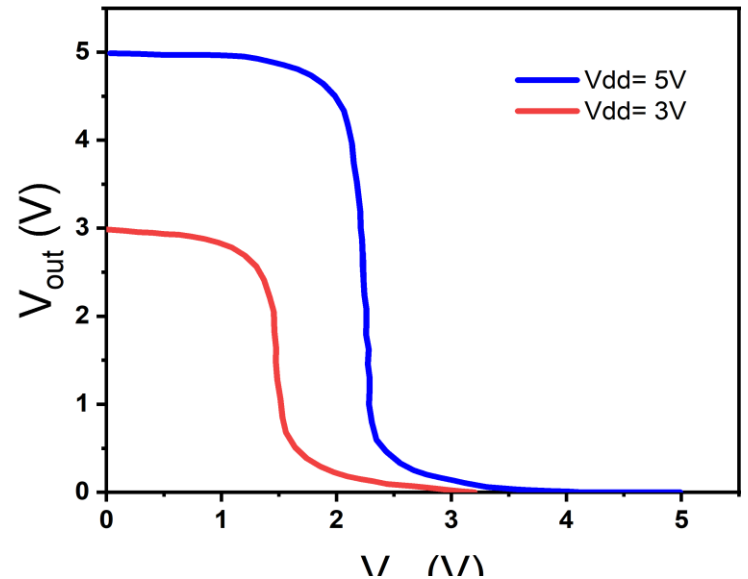
- Logic gates such as Inverters, AND, NAND, and NOR were printed
- The figures below show the fabricated logic circuits

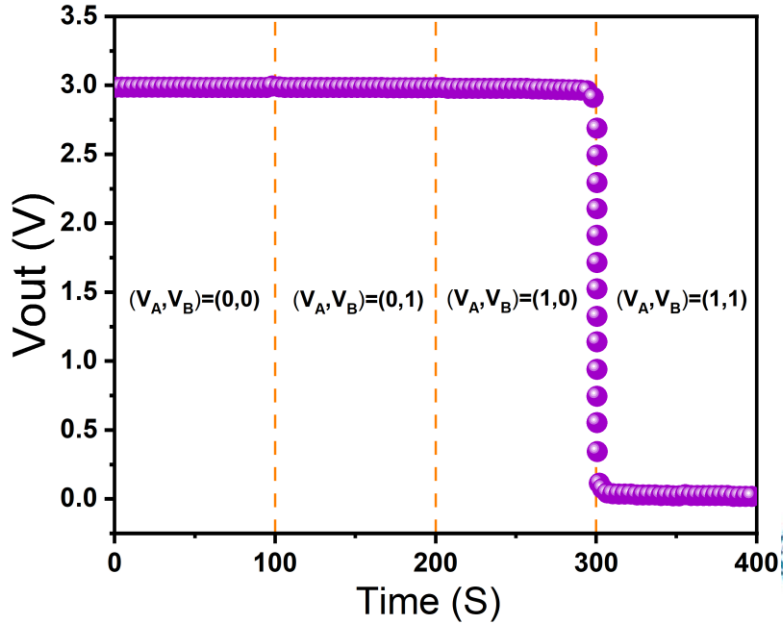




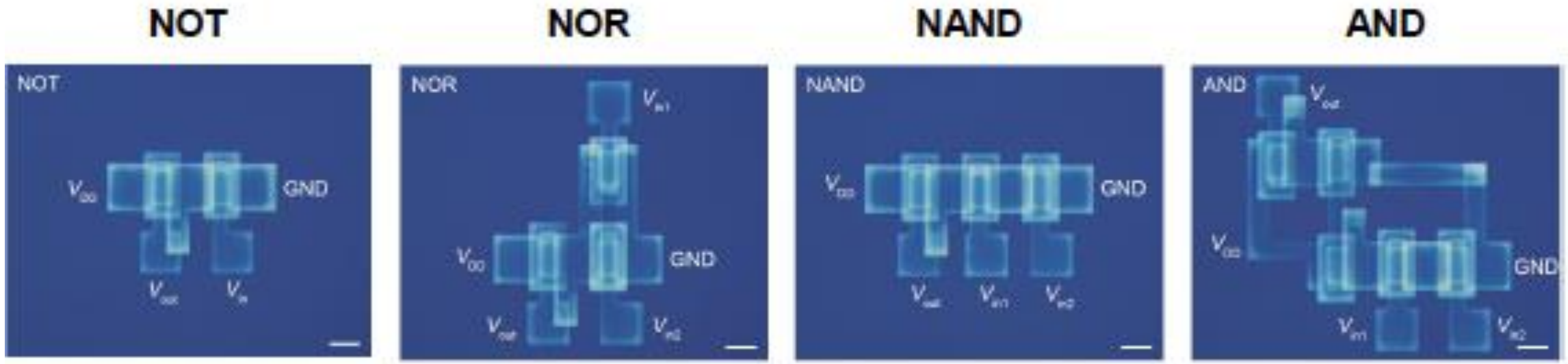


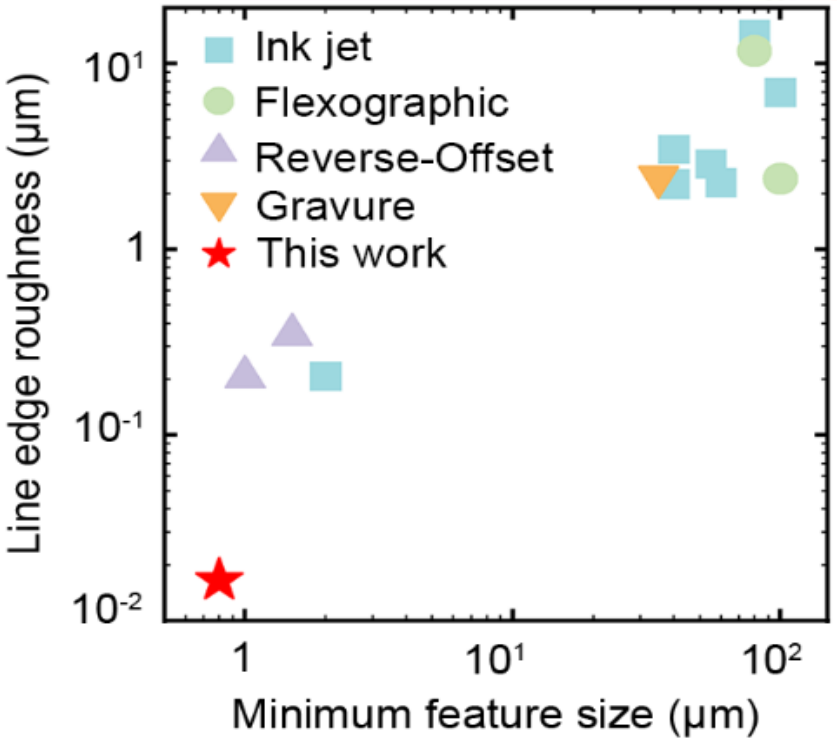


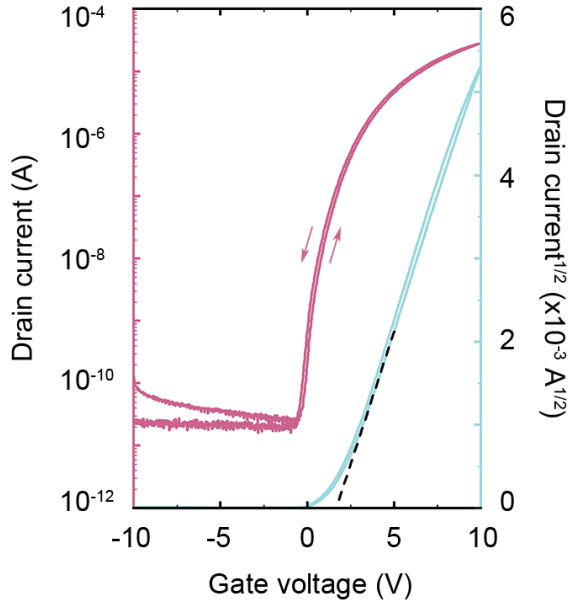


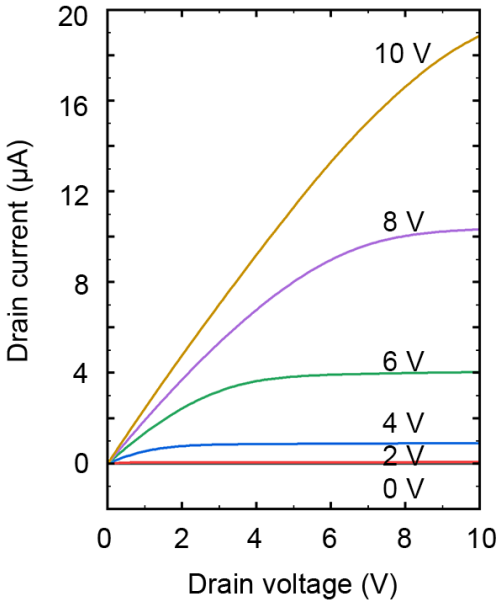


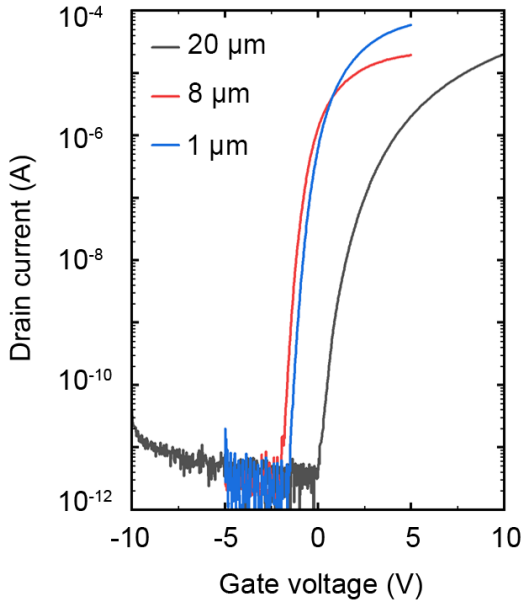
Fast Fluidic Assembly Process– FFx Platform (In_2O_3)





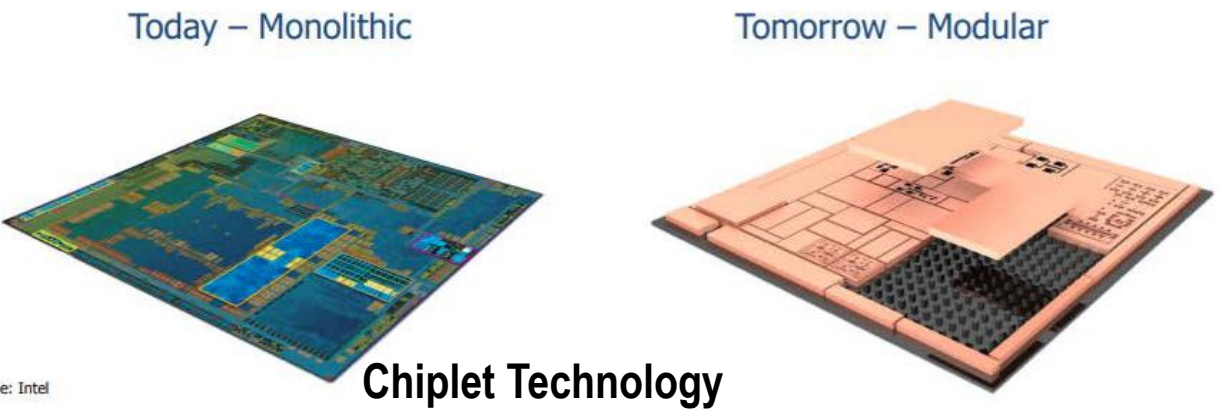






Nano PS©

Advanced Packaging for Heterogeneous Integration
for chiplet technology for integrating multiple dies in a package or system



Chiplet Technology

- **Conventional packaging approaches can not meet the resolution and density requirements.**
- **It can only be done at conventional fabs now.**

Fully automated and cyber enabled system

- **Submit DXF or GDS files and load ink, wafers, etc.**
- **Additively Manufacture:**
  - **micro and submicron interconnects.**
  - **passive components**
  - **onto silicon, glass or organic substrates (interposers)**

Nano OPS©

Sustainable Nanomanufacturing

- The energy requirements for constructing nanoscale transistors on a 1 cm² silicon substrate were compared using directed assembly and conventional fabrication methods, and the results show that at least an order of magnitude in **savings in embodied energy cost**.
- The use of the new FFx platform, a fast fluidic assembly process, is estimated to reduce manufacturing costs **by 25 times compared to conventional fabrication.**

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26th CIRP Life Cycle Engineering (LCE) Conference

Cumulative Energy Demand for Printing Nanoscale Electronics

Salman A. Abbasi, Ahmed Busnaina and Jacqueline A. Isaacs*

National Science Foundation Nanoscale Science and Engineering Center for High-Rate Nanomanufacturing
Department of Mechanical and Industrial Engineering
Northeastern University, Boston, Massachusetts 02115, USA

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The Future of Electronics Manufacturing

Any Material
Any Substrate

Minimum Feature Size
20 nm

High throughput
10 – 100x Faster

Cheaper 10 – 100x

Fab-in-a-Tool: A Fully Automated Nanoscale Electronics Manufacturing Platform

https://www.youtube.com/watch?v=QpbDfAJzXDU&t=7s

www.nano-ops.us

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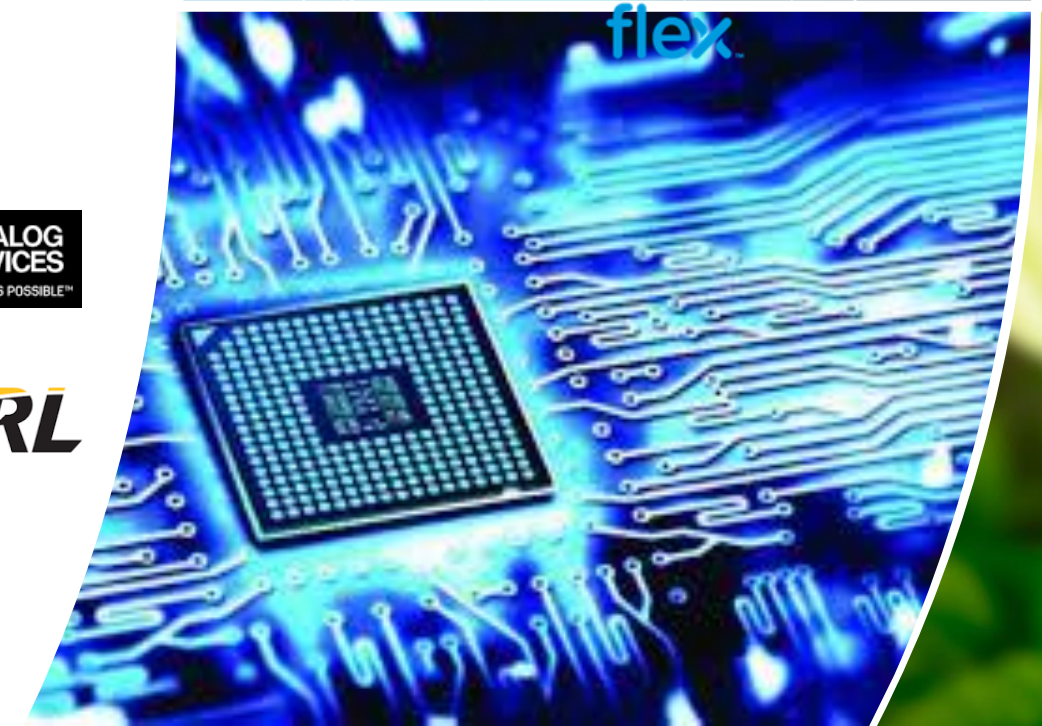
Technological Impact

- Adv. Packaging on demand
- Passive and Active components on demand
- Fast prototyping and development cycle
- Security
- Sustainable
- Material innovation



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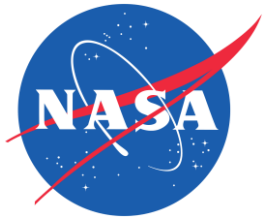

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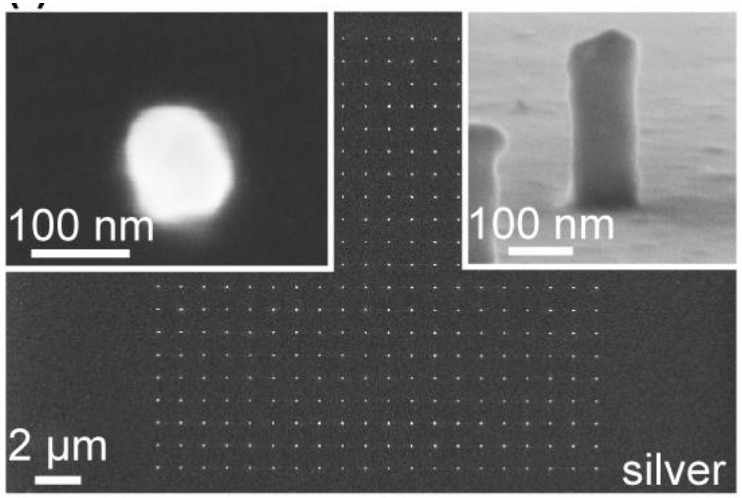
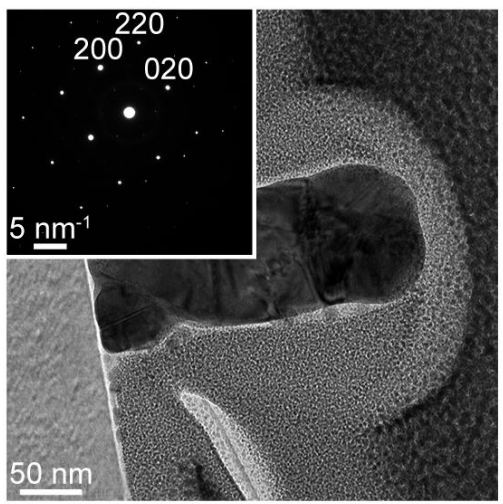
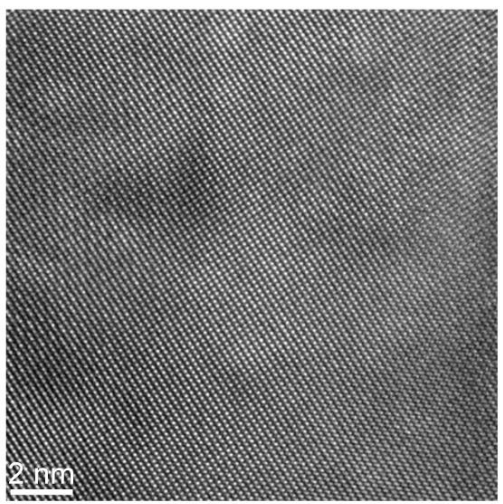
Additively Manufacturing Single Crystal Semiconductor and Metal

Interfacial convective directed assembly





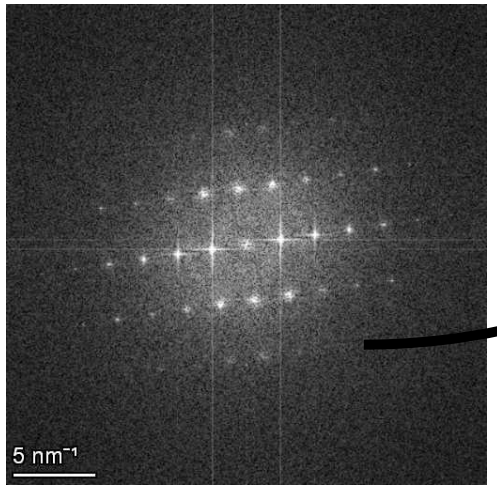


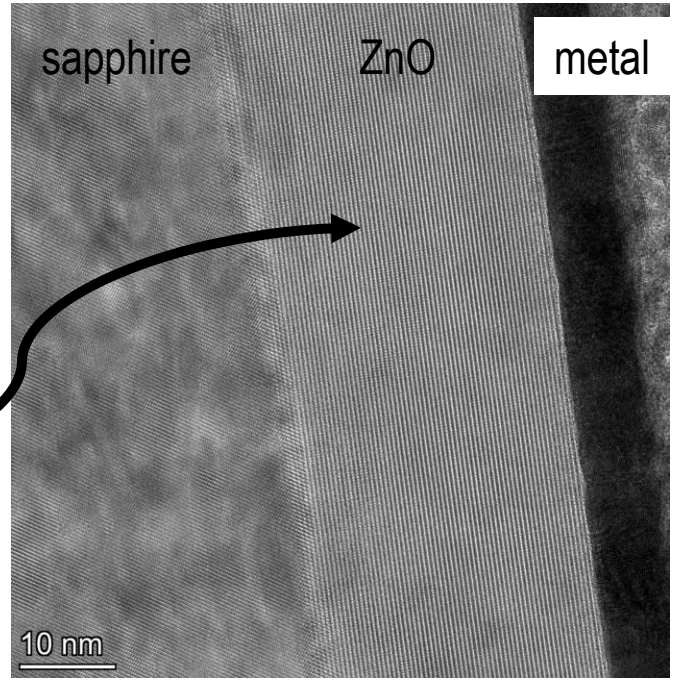
Advanced Materials, 2020.

Room temperature Printing & sintering to make wafer scale single crystal metal (Ag) nanostructures

Single Crystal TEM image of sintered assembled ZnO nanoparticles

Fast Fluidic directed assembly





RTP sintering of II-VI nanoparticles (1000 c for 2 min) on sapphire yields gives a single crystal structure throughout.

Phosphorous 3D doping profile (TOF-SIMS)